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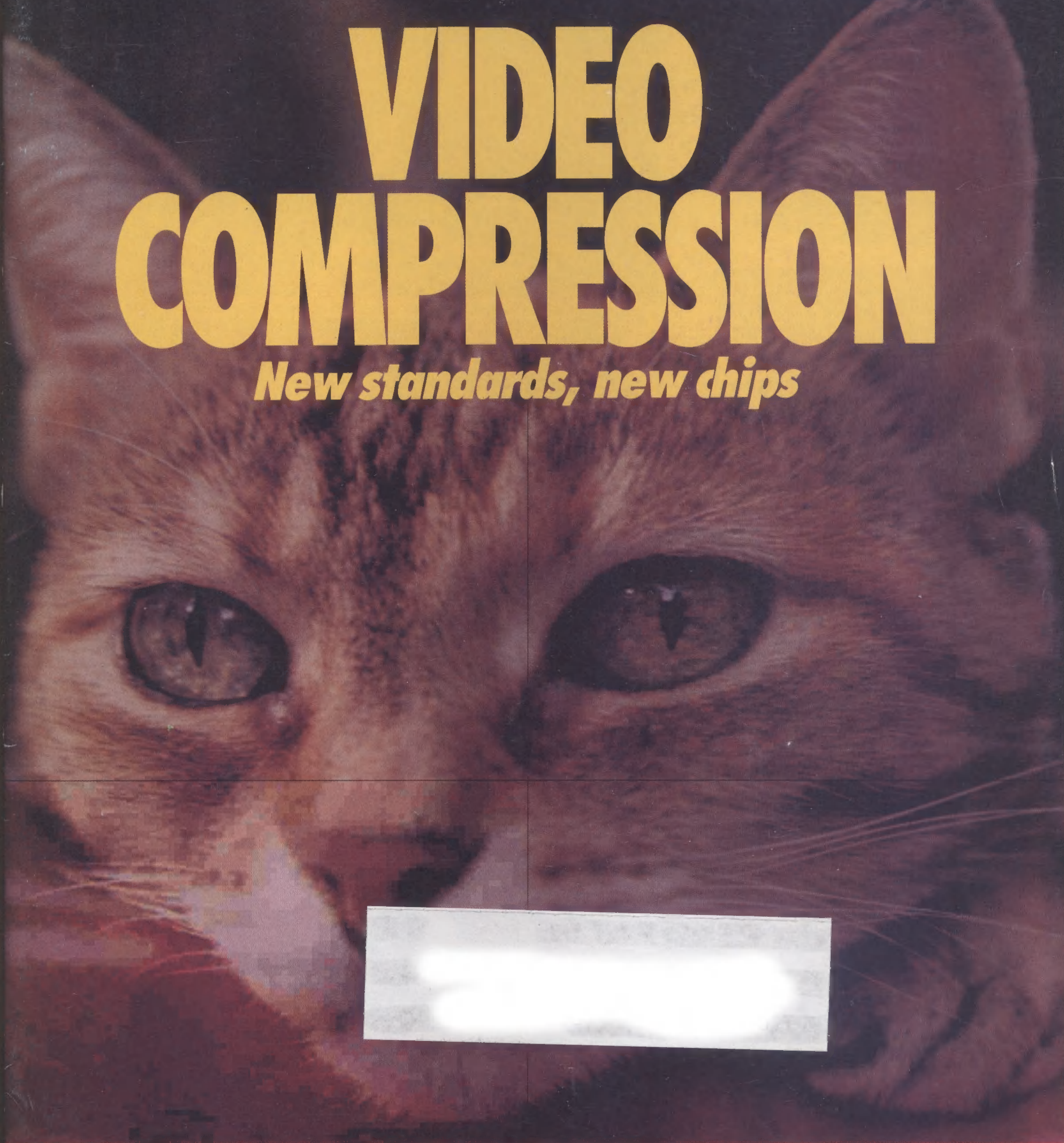

ALSO: OPTOLITHOGRAPHY FENDS OFF X-RAYS, P. 24

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SPECTRAL LINES

By DONALD CHRISTIANSEN

When a hurricane hit New York's Long Island, the power utility had in place an efficient emergency power recovery plan, but no program to tell 380 000 blacked-out customers what was going on.

APPLICATIONS

By PENG H. ANG, PETER A. RUETZ, and DAVID AULD

Compression Labs Inc.

Video compression technology embodied in new standards plus a new class of IC chip sets is likely to unleash a variety of video applications, including the conferencing system shown here.

EDUCATION

By ALEX HILLS

A master's degree program in information networking at Carnegie Mellon University includes business and public policy, as well as technical subjects like telecommunications and computers.

ADVANCED TECHNOLOGY

By GARY E. FLORES and BRUCE KIRKPATRICK

Ultraviolet lithography puts 0.5-micrometer lines on ICs in the factory, $0.35\text{-}\mu m$ lines in the laboratory. The huge investment in X-ray lithography for production can wait until 2000.

BACK TO BASICS

By JOHN D. RYDER

Though awareness of a relationship between electric charges and magnetic poles dates to the 17th century, it was Volta's battery in the 18th century that led to demonstrations of the link.

Cover: Video compression allows perfect reconstruction of an image—up to a point. Each quadrant of this cat's face was made with a different compression ratio using Visionary boards from Rapid Technology Corp., Amherst, N.Y. In quadrant 4, at the highest video compression ratio (110:1), the 8-by-8-pixel blocks are obtrusive. But pixel blocks show barely, if at all, in 2 (21:1) and 3 (80:1). Quadrant 1 has the original, uncompressed image. See p. 16. Photo: Irene Mohler; image processing: Joe Pittari.

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Forum

Laplace and Fourier transforms

I take issue with the article "Behind the Laplace transform" by Paul J. Nahin [March, p. 60]. The most severe error is his statement that "the step function has a Laplace transform, but not a Fourier transform." This is not true with the Fourier transform pair given by a number of authors—for example, by Papoulis in his book *The Fourier Integral and Its Applications*, as $U(t) = \pi\delta(\omega) + 1/j\omega$ where U(t) is the step function and $\delta(\omega)$ is the Dirac delta function.

Nahin also implies that the Fourier transform is less useful than the Laplace because of Laplace's greater generality. But the Fourier also maps convolution to multiplication and division. And for most actual computations of frequency-domain, steady-state response from transient time-domain data, the Fourier is preferred because of the existence of fast Fourier transforms (FFTs).

Nahin indicates that Laplace (and by implication Fourier) transforms will "become one of those concepts learned in engineering school but never used on the job" because of the existence of canned computer analysis programs. Running a canned program without understanding the basis for the calculations is a procedure in which good engineers should not participate.

Raymond Luebbers
University Park, Pa.

The author responds:
Luebbers is correct in observing that the Fourier transform of a step exists if one expands the idea of a *function* to include impulses. I meant that the Fourier transform *integral* itself fails to exist for a step. As to the merits of Fourier versus Laplace transforms, I fear Luebbers confused what I "implied" with what he inferred.

As to his last point, I posed the issue as a question. It was intended as a purely rhetorical device, to promote responses to a question professors are often asked these days by computer-smart students. I agree with Luebbers' position.

In response to queries about my book, *Time Machines: Time Travel in Physics, Philosophy and Science Fiction* will appear in 1992, published by the American Institute of Physics, New York.

Debatable grounding

I would like to comment on the report "Electromagnetic fields" [August 1990, p. 31] in regard to grounding systems.

The statement that in West Germany "the power neutral is not connected electrically to the other utility lines at each residence" seems not to be correct. Bonding the neutral to telephone, water, and gas piping systems, as well as to further metallic parts of the building, is mandatory according to German standards (VDE 0100, 0190).

It is difficult to conceive the Japanese system as described ("a hybrid"), since the neutral may be either bonded or not bonded, but not half-bonded.

The question of whether the "neutral return currents can [really] travel down all those utility lines" is a most important issue to be addressed by the ongoing EPRI research plan. Usually, ground return currents do follow the path of lower reactance in spite of a much lower dc resistance that adjacent grounding systems may offer.

Celso Luiz P. Mendes
São Paulo, Brazil

According to Andreas Stamm of the Technical University in Braunschweig, Germany, in rural areas where the TT-net wiring scheme is used, the power neutral is not connected to protective earth but is grounded separately. In urban areas using the TN-net, the power neutral is grounded to the protective earth. Water pipes are typically non-metallic (except in older residences) so they cannot carry neutral return currents. Gas pipes are isolated at the service entrance. These features minimize unbalanced return currents.

The description of Japan's system as a "hybrid" meant that some parts of the system use the U.S. scheme, while other parts use the German scheme. According to Seietsu Tomita of the Central Research Insitute of the Electric Power Industry in Japan, the power neutral is not grounded at the service entrance in Japan, causing all return currents to travel on the neutral conductor. According to Gregory Rauch, project manager in EPRI's electrical systems division, many factors affect the paths along which power currents return in U.S. systems. He believes that the proximity of conductors overrides the lower resistance of other grounding systems as a determinant of the return path only when service drop wires are very long.—Ed.

Credit where it's due

The portraits of experts that appeared in "The challenge of post-Gulf conflicts," September, pp. 53–7, were drawn by Barry Ross, Northampton, Mass.

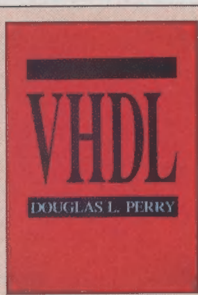
Contact: Forum, *IEEE Spectrum*, 345 East 47th St., New York, N.Y. 10017, U.S.A.; fax, 212-705-7453. The computer bulletin board number is 212-705-7308 and the password is SPECTRUM; for more information, call 212-705-7305 and ask for the Author's Guide.

Books

Coping with the electronic Tower of Babel

Larry Saunders

VHDL. *Perry, Douglas,* McGraw-Hill, New York, 1991, 458 pp., $39.95.



The U.S. Department of Defense originally developed the very high-speed integrated circuit hardware description language (VHDL) to respond to the rapidly escalating problems it had in the design and documentation of electronic parts.

Defense contractors had created a Tower of Babel by documenting thousands of electronic parts using uncounted, incompatible, and often proprietary electronic design description languages. Engineers could not understand these design descriptions because they did not know the languages. Electronic design automation (EDA) programs worked only with one or two at a time. Even the design descriptions themselves defied understanding because massive detail often obscured the overall functionality of the design.

VHDL, now an IEEE standard, will fix these problems—but only if high-quality, easy-to-use educational materials explaining the language and its use are made available. Unfortunately, most existing materials have suffered from a complex, non-engineering-oriented vocabulary. Others have focused—improperly—on the programming-language aspects of VHDL instead of on its electronic design aspects.

A really good book on VHDL would have three parts: a language tutorial; a discussion of how to design properly with VHDL—from initial specification to implementation—in a top-down design manner; and an explanation of how VHDL interacts with EDA tools, particularly in simulation, synthesis, and timing analysis.

Perry's book addresses only two of these topics. The tutorial portion is adequate, despite errors and omissions. The section on proper VHDL design is well done. But there is no useful information on EDA tool interactions with VHDL.

In general, I liked the book's structure and progression of ideas. I particularly liked the idea of teaching VHDL by example. Chapters 1 through 8, which introduce the features of VHDL, focus mainly on showing the designer "how to write concise, efficient, correct VHDL descriptions of hardware." I found this section interesting, if a little slow at first.

Unfortunately, this section has several errors, ranging from improper syntax in some VHDL statements to an erroneous description of a resolution function.

Some omissions also bothered me. There is no discussion of register and bus (guarded) signals—an effective piece of language for developing state-machine descriptions and other uses. Nor is there anything on the important subject of writing simulation test cases using VHDL.

The book's final part works through a fairly complicated design example. It moves from initial specification to final implementation in a top-down design manner. This section is probably the best reason to buy the book. Although the *why* of some of the featured design decisions is not always explained, the author does a good job showing how to lay out, partition, and refine the design example.

The section ends with a short, inadequate discussion about VHDL synthesis. Since synthesis is the primary reason that hardware description languages are enjoying such wide acceptance in the engineering community, this inadequacy is particularly troublesome.

Is this book worth reading? Overall, I believe it is. The VHDL-by-example approach is different from that in other works on VHDL, and should appeal to readers who lack the fortitude to wade through other publications. The design example in the last section is useful to those who want to learn how to code in VHDL. Regrettably, they will have to go elsewhere to learn about issues in EDA tool and design methodology.

Larry Saunders (A) is president of North Oaks EDA Consulting, Rochester, Minn. A veteran of the original VHDL contract development team in the early '80s, he was chairman of the IEEE VHDL Analysis and Standardization Group and is presently chairman of the VHDL International Users Forum.

COORDINATOR: Glenn Zorpette

Recent books

Citizen Scientist. *Hippel, Frank von,* Simon & Schuster, New York, 1991, 285 pp., $12.95.

Handbook of Microwave and Optical Components, Vol. 4. Ed. *Chang, Kai,* John Wiley & Sons, New York, 1991, 484 pp., $74.95.

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Calendar

Meetings, Conferences and Conventions

OCTOBER

International Conference on Systems, Man and Cybernetics (SMC); Oct. 13–16; Omni Charlottesville Hotel, Charlottesville, Va.; Sandra Sullivan, University of Virginia, Room A238, Thornton Hall, Charlottesville, Va. 22903; 804-924-6271.

Second International Workshop on Raster Imaging and Digital Typography (C); Oct. 14–15; Boston Park Plaza Hotel, Boston; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W, Washington, D.C. 20036; 202-371-1013; fax, 202-728-0884.

International Conference on Computer Design–ICCD '91: VLSI in Computers and Processors/MIT CAD Open House (ED); Oct. 14–16; Royal Sonesta Hotel, Cambridge, Mass.; Dwight Hill, AT&T Bell Laboratory, 3D-446, 600 Mountain Ave., Murray Hill, N.J. 07974; 908-582-7766.

10th Digital Avionics Systems Conference (AES); Oct. 14–17; Los Angeles Hilton Hotel, Los Angeles; Milt Holt, NASA Langley Research Center, Mail Stop 469, Hampton, Va. 23665; 804-864-1596; fax, 804-864-7891.

International Display Research Conference (ED); Oct. 15–17; Hyatt Islandia Hotel, San Diego, Calif.; Andras Lakatos, Xerox Corp., 800 Phillips Rd., Webster, N.Y. 14580; 716-422-9700.

International Workshop on Object Orientation in Operating Systems (C); Oct. 17–18; Hyatt Regency, Palo Alto, Calif.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

GaAs Reliability Workshop (ED); Oct. 20; Doubletree Hotel, Monterey, Calif.; Anthony Immorlica, General Electric Co., Electronics Park, Building 3, Room 155, Syracuse, N.Y. 13221; 315-456-3514.

GaAs Integrated Circuits Symposium (ED); Oct. 20–23; Monterey Sheraton Hotel, Monterey, Calif.; Suzanne Kuntz, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-347-5900.

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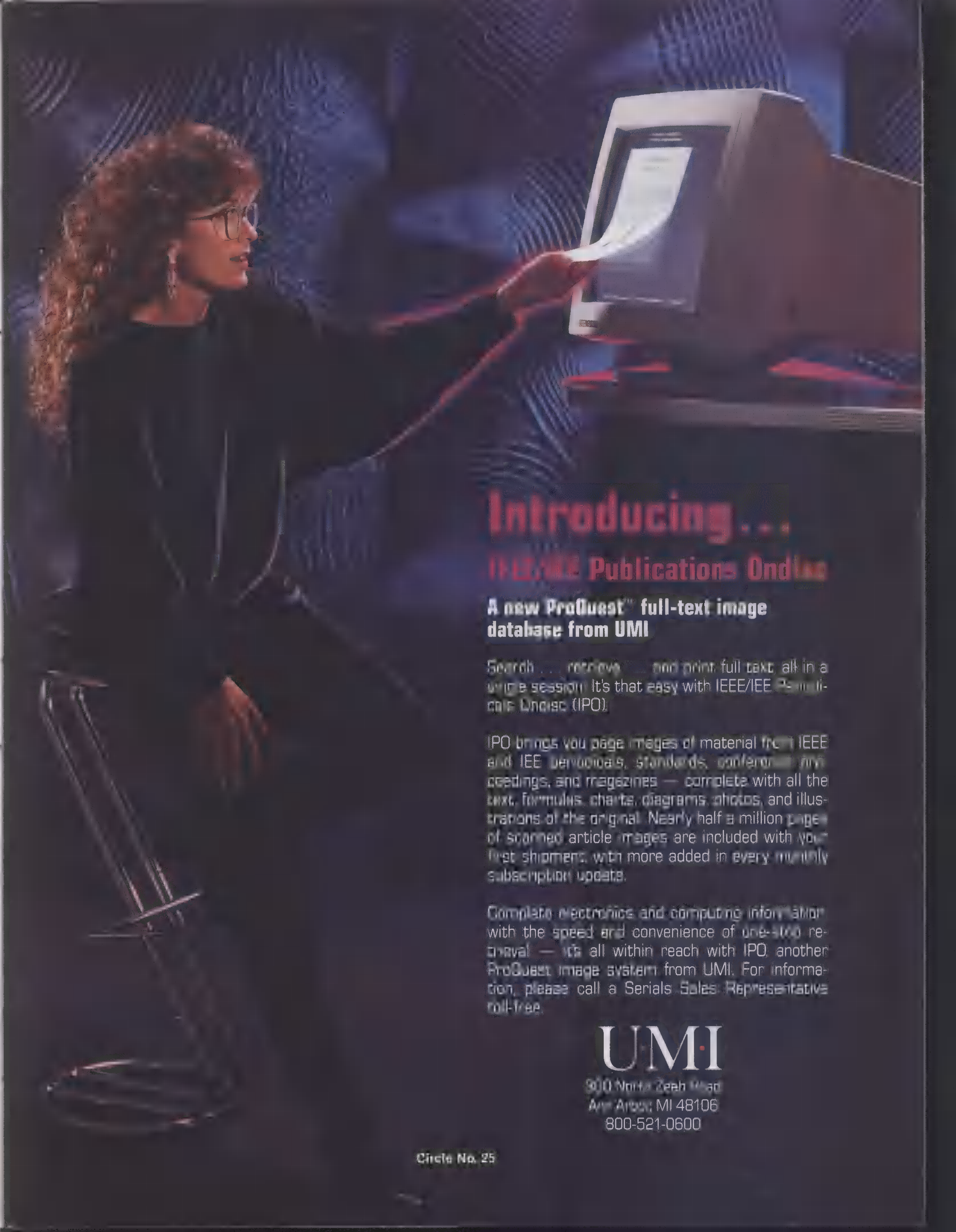

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Graphics

Great solid stuff on flat screens

The puzzle: how to render solid objects with spectacular realism, including reflections and shadows cast by shiny surfaces, spot or diffuse lighting, and shading.

One of the most popular solutions: tracing the paths of light rays, a classical technique used by artists in Renaissance Europe.

In computer graphics, however, there is a catch. Ray tracing is computationally intensive in the extreme. The reflection, absorption, and intensity of millions of rays of light must be calculated, taking into account the nature of the incident light, the positions of viewer and light sources, and the attributes of the illuminated objects.

To produce realistic-looking images, the ray-tracing process begins at the end, with the rays that reach the viewer. (Starting at the light source would entail following the many rays that never reach the viewer to find the relatively few that do.) These rays are then traced backward from the viewer's eye through a plane representing the computer monitor's screen, to the object or objects being viewed, and then on to the light source itself. Each step of the way, the computer determines how the ray is affected, for example, as it bounces off a reflective object or passes through a transparent one.

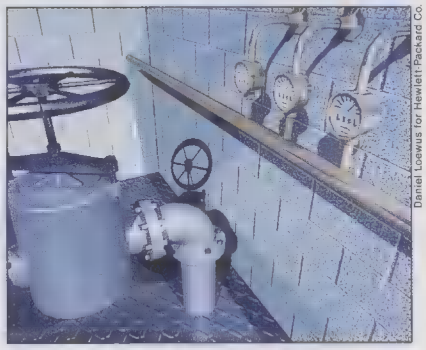
All ray-tracing algorithms search for the intersections of each ray with every object in the scene, and then scan this list of intersections, looking for the objects nearest the origin of each ray. This seemingly simple routine is performed so many times that it can occupy 95 percent or more of the total programming time.

The number of computations required quickly becomes unmanageable as the scene's complexity increases. "Two or three spheres on a checkered board is about the upper limit of what you'd want to render in this way," said Andrew S. Glassner, a graphics expert and member of the research staff at the Xerox Palo Alto Research Center in California.

Over the last decade, researchers have explored at least a half-dozen basic approaches to accelerating ray tracing. Three of the most common strategies fall under categories known as directional techniques, space subdivision (pioneered by Glassner), and hierarchical boundary volumes. Glassner noted that virtually all methods of accelerating ray tracing so far devised have the same goal: reducing the length and complexity of the answer to the question, "Given a ray and a scene, what is the first object intersected by that ray?" This answer is critical because any rendering technique must begin by determining what objects are visible to the viewer.

The basic strategy is reducing the number of objects that *could be* the first one struck by the ray to a manageable candidate set, which definitely includes the object first struck by the ray.

With hierarchical boundary volumes, the scene is divided into a series of imaginary, nesting boxes. An image of a bookshelf, for example, has a box around the whole unit.



Daniel Loewus for Hewlett-Packard Co.

Rendering of this ray-traced image, notable for the texture on the floor, brick walls, and gray valve casing at left, was accelerated with the hierarchical boundary volume technique. The texture, also known as bump mapping, is easily created with ray tracing by varying the angles of the light reflected by the surface at each point.

Within this big box are boxes for each shelf; within each of these are smaller ones around groups of books; within these smaller boxes are still smaller ones for each book.

For each ray entering the scene, the first test is whether the ray intersects with the biggest box. If the answer is no, thousands, perhaps millions of individual tests involving that ray and the myriad surfaces in the box are avoided.

If the answer is yes, progressively smaller boxes are tested until the object first struck by the ray is found. In this technique, each box is a candidate set, and as the search proceeds from large to little box, the candidate set becomes proportionately smaller.

Space subdivision methods also build candidate sets through the use of nesting boxes. However, rays are traced through these boxes, and only the objects encountered within each box are tested.

Directional methods generalize both of the basic strategies by including the direction of the ray as one of the criteria for building candidate sets.

COORDINATOR: Glenn Zorpette
CONSULTANT: Andrew S. Glassner, Xerox Palo Alto Research Center (PARC)

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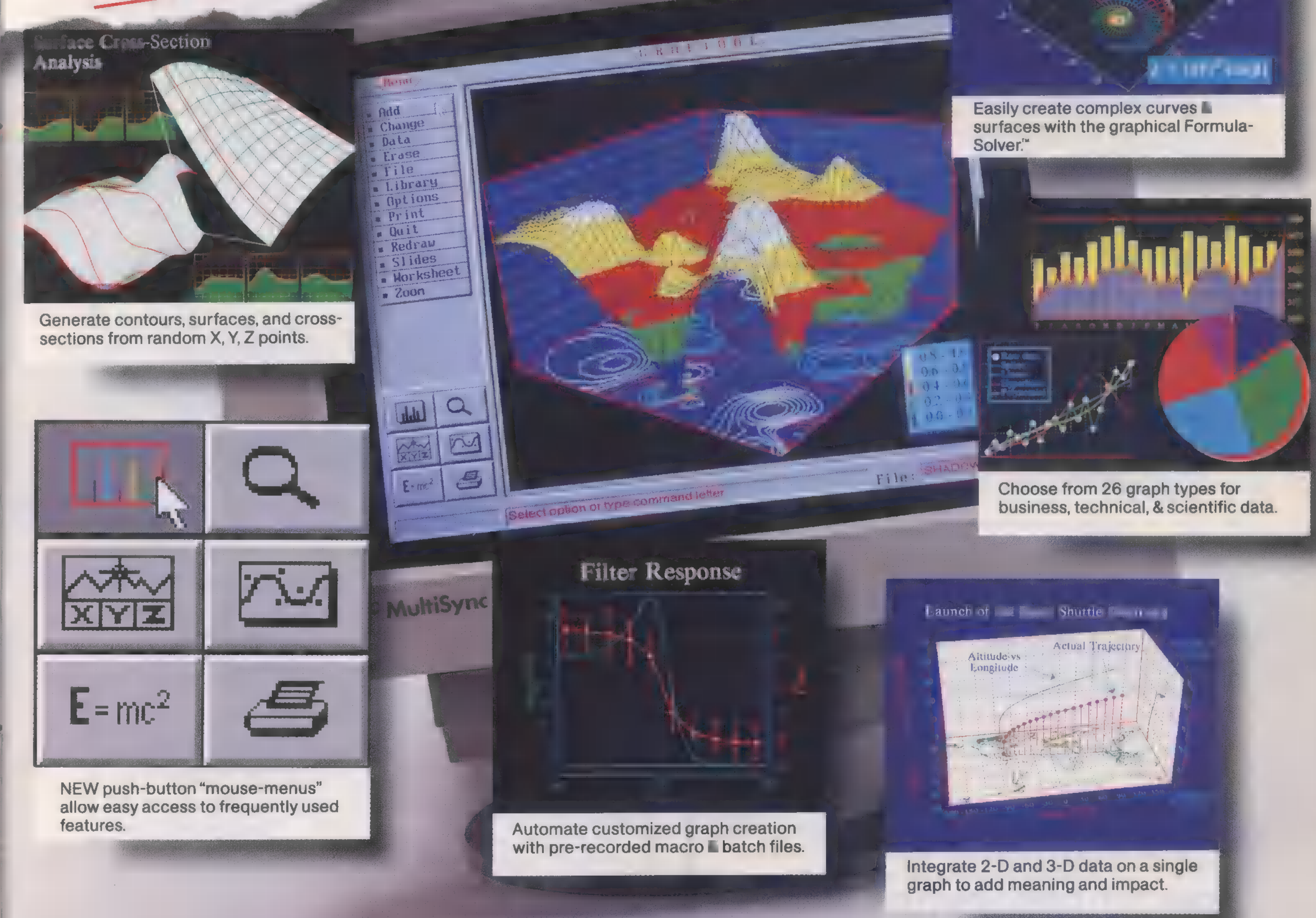

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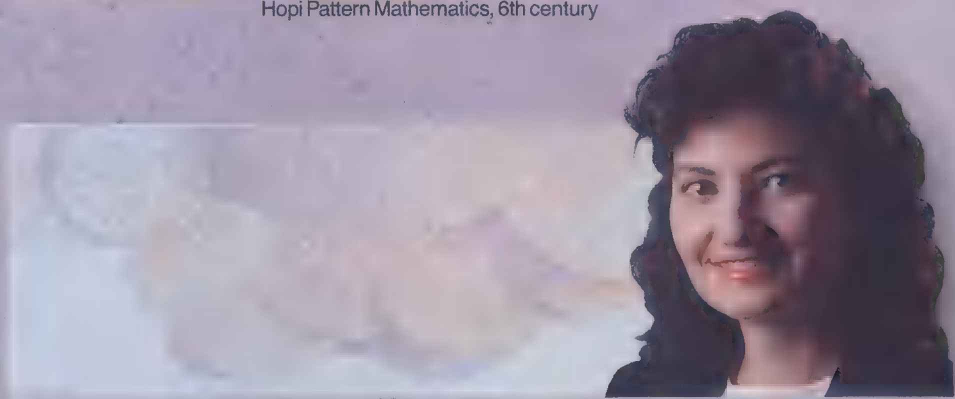

Hohokam Acid-Based Etching, 10th century

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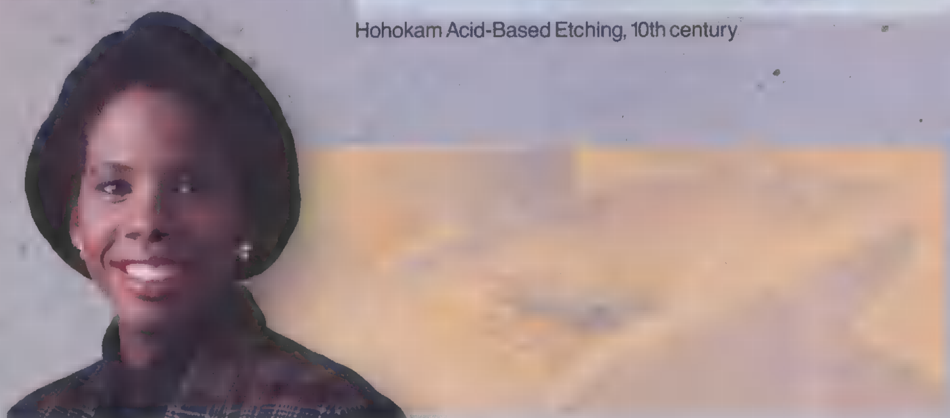

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Calendar

(Continued from p. 8)

Vehicle Navigation and Information Systems Conference–VNIS '91 (VT); Oct. 20–23; Hyatt Regency, Dearborn, Mich.; M. Krage, General Motors Research Laboratories, Department 18, 30500 Mound Rd., Warren, Mich. 48090; 313-986-2976.

Workshop on Applications of Signal Processing to Audio and Acoustics (SP); Oct. 20–23; Mohonk Mountain House, New Paltz, N.Y.; James Kates, City University of New York, Graduate Center, Room 901, 33 W. 42nd St., New York, N.Y. 10036; 212-642-2179; fax, 212-642-2379.

Conference on Electrical Insulation and Dielectric Phenomena (DEI); Oct. 20–24; Hyatt Regency Hotel, Knoxville, Tenn.; G. Edward Johnson, Room 7D-214, AT&T Laboratories, Murray Hill, N.J. 07974; 908-582-2585; fax, 908-582-5570.

Advanced Semiconductor Manufacturing Conference and Workshop (ED); Oct. 21–22; World Trade Center, Boston; Margaret Bachmeyer, 2000 L St., N.W., Suite 200, Washington, D.C. 20036; 202-457-9584.

Sixth IEEE Workshop on Computer Communications (COM); Oct. 22–24; Monterey Plaza Hotel, Monterey, Calif.; Nachum Shacham, SRI International, 333 Ravenswood Avenue, Menlo Park, California 94025; 415-859-5710; fax, 415-859-4812.

Visualization '91 (C); Oct. 22–25; Marriot Mission Valley, San Diego, Calif.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036; 202-371-1013; fax, 202-728-0884.

International Test Conference (C); Oct. 26–30; Opryland Hotel, Nashville, Tenn.; Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

14th International Congress on Instrumentation in Aerospace Simulation Facilities–ICIASF '91 (AES); Oct. 27–30; Holiday Inn Crowne Plaza, Rockville, Md.; William Yanta, Naval Surface Warfare Center, K24, 10901 New Hampshire Ave., Silver Spring, Md. 20903-5000; 301-394-1928.

Portland International Conference on Management of Engineering and Technology–Picmet '91 (EM); Oct. 27–31; Marriott Hotel, Portland, Ore.; Dundar F. Kocaoglu, Portland State University, Engineering Management Program, Portland, Ore. 97207; 503-725-4660; fax, 503-725-4667.

Eighth International Conference on Automotive Electronics (VT); Oct. 28–31; Savoy Place, London; Jane Chopping, Conference Organizer, IEE Conference Services, Savoy Place, London WC2R OBL, England; (44+1) 240 1871, ext. 218.

International Logic Programming Symposium (C); Oct. 29–Nov. 2; San Diego Princess, San Diego, Calif.; IEEE Computer Society Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

International Professional Communication Conference–IPCC '91 (PC); Oct. 30–Nov. 1; Sheraton World Resort, Orlando, Fla.; Daniel Plung, Westinghouse Savannah River Co. , 1070 Silver Bluff Rd., Aiken, S.C. 29801; 803-642-4066.

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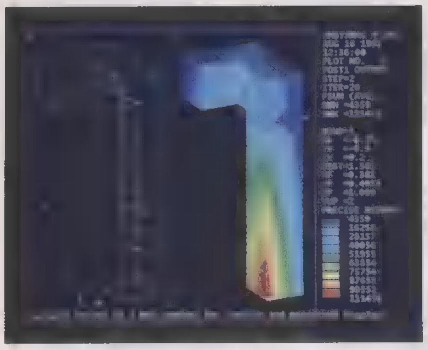
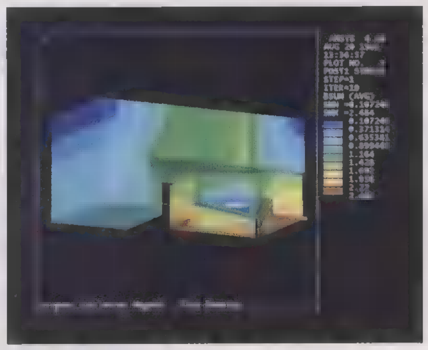
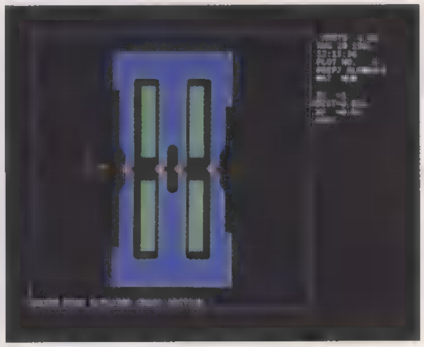


ANSYS magnetics was used by Stone and Webster Engineering Corporation with MIT Plasma Fusion Center to analyze the conductors, iron mass, and field in a MHD channel. Displayed are the Lorentz forces in a conductor.



Magnetic field analysis for a cyclotron magnet design was performed by the National Superconducting Cyclotron Laboratory, Michigan State University, using ANSYS magnetics to determine flux density levels.



A printer head linear actuator device was modeled by IBM Corporation to evaluate normal end axial forces on a sliding armature situated between two stators.

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Circle No. 36

Spectral lines

OCTOBER 1991 Volume 28 Number 10

Power consumers in the dark

In civil emergencies, keeping the affected populace informed is high on the agenda if casualties and hardships are to be held to a minimum, and if normalcy is to be restored quickly and efficiently.

When Hurricane Bob struck New York's Long Island in August, despite 24 hours or more of warning, it caught the power utility (Lilco), the telephone company (New York Telephone), and numerous local radio stations short, or out of practice, in communicating with the public.

Lilco, embarrassed by shortcomings in previous emergencies, notably Hurricane Gloria in 1985, had an emergency restoration plan in place that evidently worked well, except for letting the populace know what was going on.

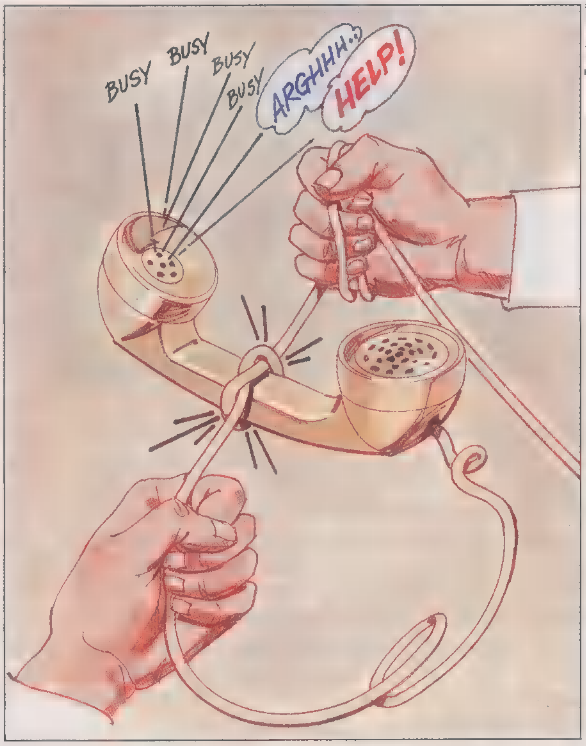
In some aspects, the plan worked better than expected. Hurricane Bob nipped the eastern end of Long Island and left 380 000 customers without power, some for as long as six days. But power for most customers was restored within five days, rather than the seven projected when the storm first hit. An account in the *New York Times* linked the repair schedule to a "carefully planned drill put into place after Hurricane Gloria."

A report on the response to the storm is now being prepared by the New York State Disaster Preparedness Commission. Its chairman, Thomas Jorling, has already affirmed "a much more rapid restoration of power following Bob than Gloria." But Richard Kessel, executive director of the New York State Consumer Board, said that while Lilco did a better job this time, the system is still vulnerable. He asked what the outcome would have been if Hurricane Bob had hit head-on. Kessel gave Lilco a B-minus for its performance during Hurricane Bob, compared to an F during Hurricane Gloria.

By the time all 380 000 customers were back on line, Lilco had picked these numbers out of its computer: 1041 repair crews replaced 219 transformers and restrung 74 miles of wire and cable; working 16-hour shifts, they erected 214 utility poles and replaced 2313 fuses; and in the process they used 21 737 connectors, 3851 clamps, and 421 cross arms. Crews from other utilities in New York, New Jersey, and Pennsylvania also helped out.

But the big criticism came from customers who were unsuccessful when they tried to reach a Lilco emergency number. Some reported hundreds of attempts (relatively easy with automatic re-dial).

Most of the 159 000 callers who did get through between Monday, when the storm hit, and Sunday called early in the week. But the bulk of those who failed were most likely those who called in the first day or so, too.



Tony Leonardi

Those who did get through, however, were not given very useful information, according to a Lilco spokesman. Lilco found that conducting repairs on a decentralized basis seemed to work well, but information about the progress of the work seldom made its way back to the centralized headquarters where the emergency telephone operators are located.

A caller who failed to get through using a Lilco emergency number called New York Telephone to see if any extra lines were being installed to handle the overload. The phone operator was unable to respond. In fact, unbeknownst to the operator, "scores" of extra lines to Lilco's emergency call center in Suffolk County were being set up. At least three additional emergency numbers were available for use, but were unknown to customers until they were published in Thursday's newspapers. And no customers to whom we talked heard them announced by newscasters.

Radio stations sampled by customers without power seemed to offer little but general storm-related information—the usual "stay away from downed power lines" and the "hardest hit and most remote areas will be last to be restored."

On the positive side, a Lilco spokesperson gave Lilco's own employees an A+ for efforts during the emergency, and most consumers seemed to concur. It was the public communications management system that got the F this time around.

Donald Christiansen

Video compression makes big gains

New standards for video compression plus new IC chips will change the world of computing, broadcasting, and communication

Digitally encoded video is upon us. Just as audio compact discs have revolutionized the recording industry, so this new technology promises to unleash a whole slew of video applications—among them, the digital laserdisc, electronic camera, videophone and -conferencing system, image and interactive video tools on personal computers and workstations, program delivery on cable and satellite, and high-definition television (HDTV). Unlike the digital audio technology of the '80s, however, many of the applications of digital video hinge on the use of data compression. The audio bandwidth, after all, is about 20 kHz, which translates into a digital data rate of about 1.4 megabits per second for high-quality stereo sound. Sampled video source signals, on the other hand, require much higher bit rates, ranging from 10 Mb/s for broadcast-quality video to more than 100 Mb/s for HDTV signals.

Even when still pictures are involved, as in image archival systems, a mountain of data is needed to represent them. For example, a color image with resolution of 1000 by 1000 picture elements (pixels) at 24 bits each will occupy 3 megabytes of storage in an uncompressed form. This will not fit onto a high-density floppy diskette, which can hold just 1.2 Mbytes.

Meanwhile, to facilitate industry growth, three standards are being developed for still and moving pictures and for videoconferencing. Sets of chips already exist for all three purposes, some of them proprietary designs, and others in agreement with the standards closest to completion.

HOW IT WORKS. Compression methods build on both redundancies in the data and the nonlinearities of human vision. They exploit correlation in space for still images and in both space and time for video signals. Compression in space is known as intra-frame compression, while compression in time is called inter-frame compression. Generally, methods that achieve high compression ratios (10:1 to 50:1 for images and 50:1 to 200:1 for video) are lossy in that the reconstructed data are not identical to the original.

Peng H. Ang, Peter A. Ruetz, and David Auld
LSI Logic Corp.

Lossless methods do exist, but their compression ratios are far lower, perhaps no better than 3:1. Such techniques are used only in sensitive applications such as medical images. For example, artifacts introduced by a lossy algorithm into an X-ray radiograph may suggest an incorrect interpretation and alter the diagnosis of a medical condition. Conversely, for commercial, industrial and consumer applications, lossy algorithms are preferred because they save on storage and communication bandwidth.

These lossy algorithms also generally exploit aspects of the human visual system. For instance, the eye is much more receptive to fine detail in the luminance (or brightness) signal than in the chrominance (or color) signals. Consequently, the luminance signal is usually sampled at a higher spatial resolution. (For example, in broadcast quality television, the digital resolution of the sampled luminance signal is 720 by 480 pixels, while for the color signals it may be only 360 by 240 pixels.) Second, the encoded (or compressed) representation of the luminance signal is assigned more bits (a higher dynamic range) than are the chrominance signals.

Video data, even after 100:1 compression, can be decompressed with close to analog videotape quality

Also, the eye is less sensitive to energy with high spatial frequency than with low spatial frequency. Indeed, if an image on a 13-inch personal computer monitor were formed by an alternating spatial signal of black and white, the human viewer would see a uniform gray instead of the alternating checkerboard pattern. This deficiency is exploited by coding the high-frequency coefficients with fewer bits and the low ones with more bits.

All these techniques add up to powerful lossy compression algorithms. In many subjective tests, reconstructed images that were encoded with a 20:1 compression ratio are hard to distinguish from the original. Video data, even after compression at ratios at 100:1, can be decompressed with close to analog videotape quality.

STANDARDS. Lack of open standards could slow the growth of this technology and its applications. Three digital video standards that have been proposed are the Joint Photographic Experts Group (JPEG) standard for still picture compression; the Consultative Committee on International Telephony and Telegraphy (CCITT) Recommendation H.261 for video teleconferencing; and the Moving Pictures Experts Group (MPEG) for full-motion compression on digital storage media (DSM).

JPEG's proposed standard is a still-picture–coding algorithm developed by a research team under the auspices of the International Standards Organization (ISO). The team convened in 1987 and the algorithm is currently an ISO committee draft 10918 recommendation. The scope of the algorithm is broad: it comprises a baseline lossy approach and an extended lossless approach, as well as independent functions using coding techniques different from the baseline one. Only the first approach will be discussed here.

The JPEG baseline algorithm falls under the heading of transform-based image coding. A color image can be represented in different color systems. Those in wide use today include R-G-B (the three primary colors red, green, and blue) in the computer industry; Y-U-V (Y for luminance or brightness, U and V for color difference signals Y-R and Y-B, respectively) in the television industry; and C-M-Y-K (cyan, magenta, yellow, and black) in the printing industry. Within each color system, the constituent parts are called components. Thus, there are three color components in the R-G-B system, four in the C-M-Y-K system.

Each component of the source image in the JPEG encoder and decoder is divided into non-overlapping blocks of 8 by 8 pixels [Fig. 1]. Each block is then transformed using the two-dimensional discrete cosine transform (DCT) with an 8-by-8 kernel.

The resulting 64 coefficients, computed as a 2-D array of 8-by-8 numbers, represent the frequency contents of the given block. The DCT coefficient value in the upper left-

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hand corner of the 2-D array measures the energy of the zero-frequency or direct current (dc) term. (For example, if the original 8-by-8 image has a constant value, then only the dc term in the transformed space is nonzero.) The other 63 entries are alternating current (ac) coefficients; they give the relative strengths of signal terms with increasing horizontal frequency from left to right and for terms with increasing vertical frequency from top to bottom.

Next, the DCT coefficients are quantized. The quantization step size varies with frequency and component. The dependence on frequency reflects the fact that the high-frequency coefficients subjectively matter less than the low-frequency ones and may therefore be quantized with a larger step size (that is, more coarsely). In addition, an individual component may have its own quantization table. In the committee draft of the JPEG algorithm, up to four quantization tables are allowed.

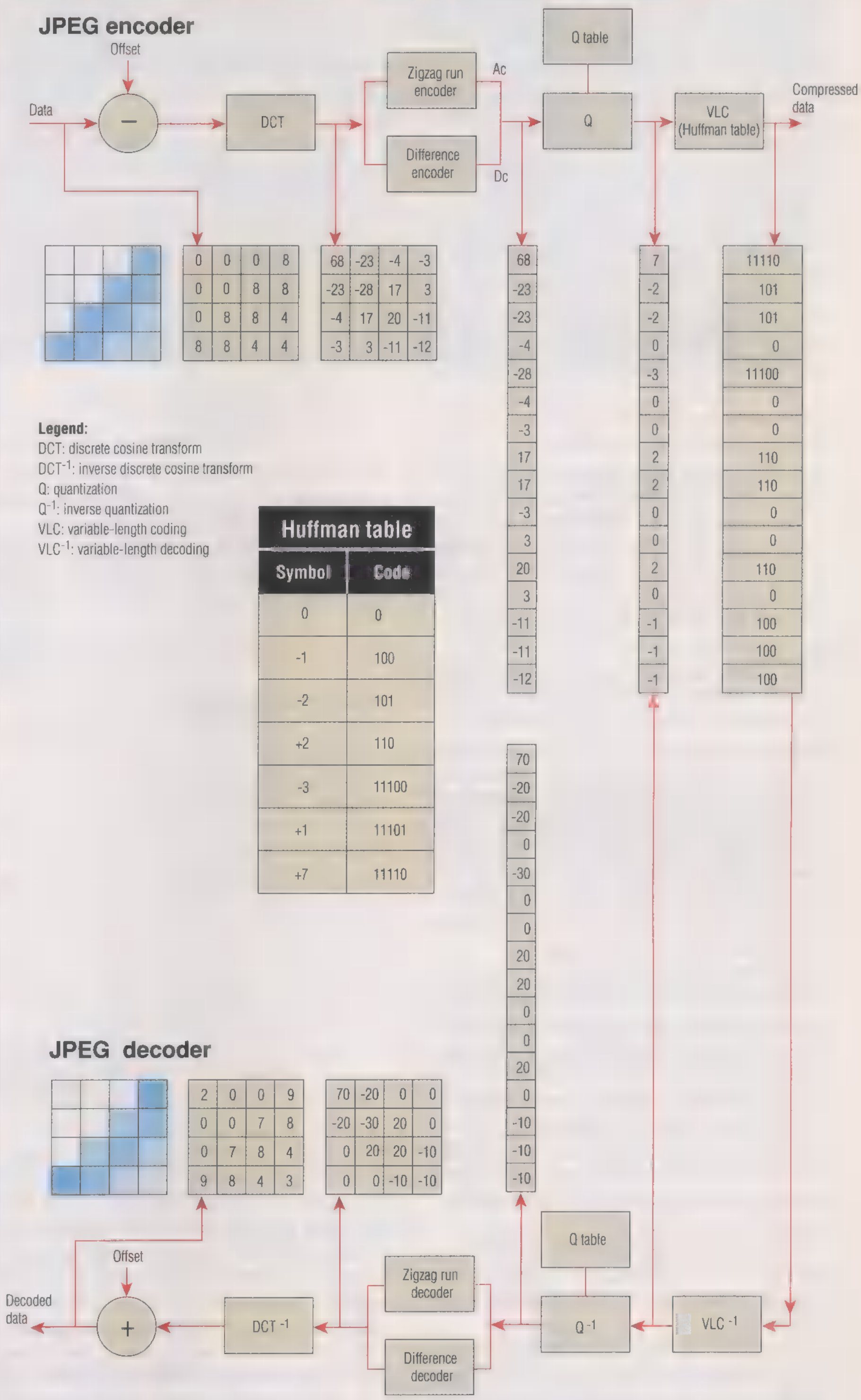
Following quantization, the coefficients are re-ordered into a one-dimensional array by reading out the entries of the two-dimensional array along a zigzag route. In this way, the quantized coefficients are "approximately" arranged in order of ascending frequency.

Next, the dc and ac coefficients are loss-

Defining terms

Discrete cosine transform (DCT): conversion of time-domain into frequency-domain data.
Entropy coding: an efficient coding method that encodes frequent events with fewer bits than it does infrequent events.
Huffman coding: a type of entropy coding that uses predetermined variable-length code words.
Inverse discrete cosine transform (DCT^{-1}): data conversion from the frequency into the spatial domain.
Inverse quantization: scaling up of previously quantized data into larger-range numbers.
Joint Photographic Experts Group (JPEG): a group of engineers and scientists from many companies worldwide seeking to formulate a standard method for the compression and decompression of still-frame, continuous-tone, photographic (gray-scale or color), digitized images.
Moving Pictures Experts Group (MPEG): a group of industry experts seeking a standard for coded representation of video and associated audio for digital storage media.
Predictive coding: the coding of each pixel by quantizing the difference between its current value and a predicted value, computed from past values.
Quantization: a process whereby data represented by many bits is scaled down to a lower-precision value requiring fewer bits.
Transform coding: mapping (or transforming) pixels of images from one domain (spatial, say) into another (such as frequency).
Variable-length coding: encoding so as to create code words of variable number of bits [see Huffman coding].
Variable-length decoding: decoding of code words of variable length into raw data.

Joint Photographic Experts Group encoder and decoder



[1] The baseline algorithm for the compression of still images included in the Joint Photographic Experts Group (JPEG) proposed standard divides the image into 8-by-8 pixel blocks, represented here by a 4-by-4 block for simplicity. In the encoder, the 16-level gray-scale image is first digitized, then undergoes a discrete cosine transform (DCT) that yields 16 frequency coefficients. The two-dimensional array is read in a zigzag fashion to reorder it into a linear array. The coefficients obtained by quantization—here just dividing by 10—are then coded using the Huffman table, shown here in a simplified version.

The decoding path takes the variable-length coding (VLC) output as input and recovers the quantized coefficients, multiplies each by 10 (inverse quantization) and turns the linear array into a 2-D one through an inverse zigzag operation. An inverse DCT operation subsequently yields a 40-bit image, representing a compression ratio of 1.6:1 here. Much higher ratios can typically be achieved.

lessly encoded, both using Huffman-style coding but keyed with different parameters. Huffman coding is a well-known means of reducing the number of bits needed to represent a data set without losing any information. The dc coefficients are differentially encoded so that the dc coefficient of the previous 8-by-8 block of the same component is used to predict the dc coefficient of the current 8-by-8 block and the difference between these two dc terms is encoded. The Huffman code table for the dc term is based on the difference values.

The zigzag-coded ac coefficients are first run-length coded. This process reduces each 8-by-8 block of DCT coefficients to a number of events. Each event represents a nonzero coefficient and the number of preceding zero coefficients. Since the high-frequency coefficients are more likely to be zero, Huffman-coding these events makes it possible to achieve efficient compression.

The JPEG baseline algorithm provides for up to two tables each for dc and ac coefficient coding. In JPEG decoding, the encoding algorithm is simply run in reverse, and it is therefore commonly described as a symmetric algorithm.

As for videotelephony, the CCITT Recommendation H.261 specifies a method of communication for visual telephony. It is often called the p*64 standard because the data rate on the communication channel is p times 64 kilobits per second, where p is a positive integer less than or equal to 32. For p=1, then, a low-quality video signal for use in picture phones can be transmitted over a 64-kb/s line. If p=32, a high-quality video signal for teleconferencing can be transmitted over a 2-Mb/s line.

The standard specifies the organization and interpretation of the transmitted bits so that two coder-decoders (codecs) from different manufacturers may successfully establish a videoconferencing session. A CCITT encoder is more complicated than the JPEG encoder, although one can distinguish familiar functional blocks such as the DCT and the quantizer [Fig. 2, top]. The decoder, however, is less complex [Fig. 2, bottom].

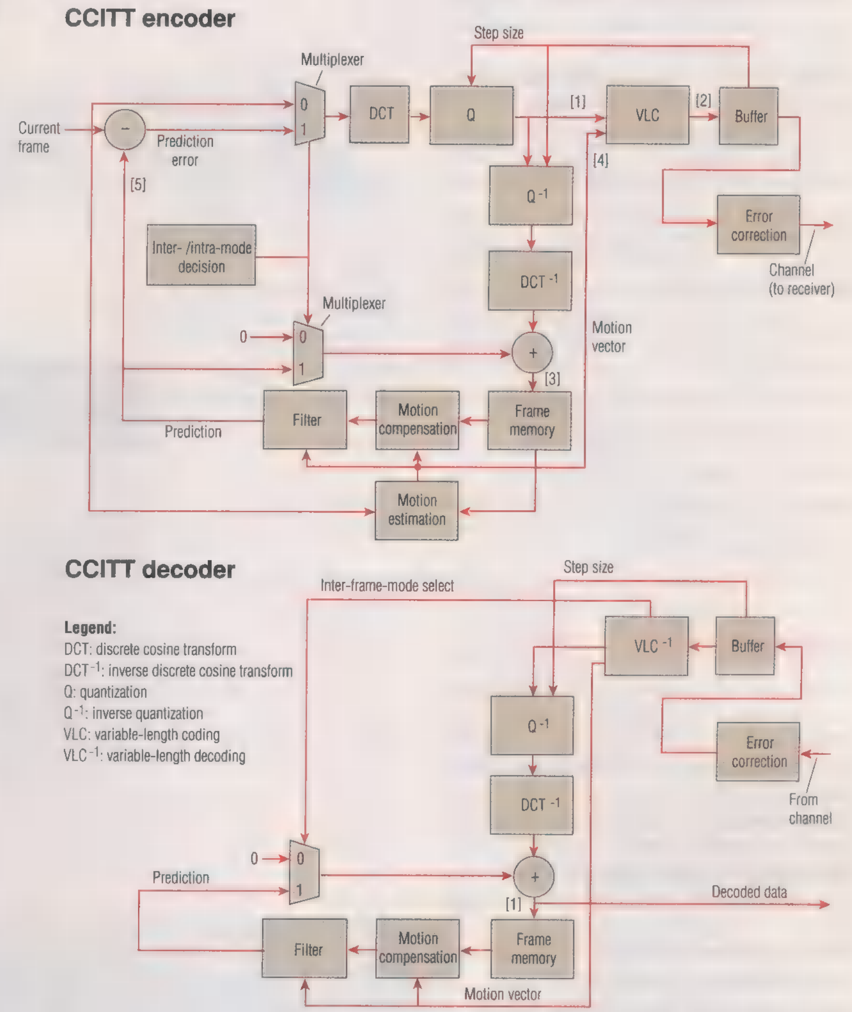
A detailed description of the baseline algorithm is beyond the scope of this article. Instead, an overview of the techniques used will be given.

The CCITT coder is called hybrid because it combines transform coding—it is also DCT-based—with predictive coding, in which a block in the current frame is predicted from a block in the previous frame using a feedback loop. (In contrast, the JPEG algorithm basically operates in an open loop and is reset at the end of each image.) It is this inter-frame prediction that results in a higher compression ratio.

Also, instead of basing predictive coding purely on the difference between the current frame and the reconstructed image in the frame memory, the CCITT H.261 standard has an optional specification for motion compensation. This increases the predictive coder's efficiency at tracking the inter-frame motion and hence its success at bit rate reduction.

PROPOSED FULL-MOTION STANDARD. Like H.261, the MPEG proposed standard is a full-motion compression algorithm with both intra- and inter-frame modes. Unlike H.261, the data rate may not exceed the 1.5 Mb/s of today's digital storage media. (There are ongoing development efforts to increase the data transfer rate for next-generation media.) Present media include compact disc drives, digital audio tape (DAT) drives, and magnetic hard disks.

The standards committee for MPEG has



[2] The first of a sequence of frames is intracoded in the full motion compression scheme proposed by the Consultative Committee for International Telegraphy and Telephony (CCITT). Like JPEG, each 8-by-8-pixel block of the frame is encoded with the discrete cosine transform (DCT) and then quantized (top). At point [1], there are two signal paths: one leads toward a receiver through a lossless coder and optional error-correction circuitry; the other—a feedback—is inverse quantized and undergoes inverse DCT to yield a reconstructed block for storage in frame memory. Reconstruction is needed because inter-frame compression uses predictive coding, which requires the encoder to track the behavior of the decoder to prevent the decoder's reconstructed image from diverging from the original input. The coder can be bypassed (instead of the signal being taken at [2]) because it is lossless and without influence on the reconstruction process. When the entire frame has been processed, a reconstructed image as seen by the decoder is stored in the frame memory at [3]. Next, inter-frame coding is applied. To compensate for motion, each 8-by-8 block in the current frame is matched with a search window in the frame memory. Then the motion vector that represents the offset between the current block and a block in the prior reconstructed image that form the best match [4] is coded and sent to the receiver. The predictor at [5] gives the motion-compensated 8-by-8 block from the reconstructed frame. The difference between this and the original block is transform coded, quantized and coded before being sent to the receiver. The CCITT decoder (bottom) first corrects incoming bit stream errors, and then decodes the data in the variable-length decoder. Passage through the inverse quantizer and the inverse DCT yields the DCT coefficients. At [1], a block like one in the encoder's feedback loop has been reconstructed and stored in the frame memory. In inter-frame mode, motion vectors extracted from the variable-length decoder are used to provide the location of the predicted blocks.

not completed its work and the system and audio specifications remain in flux. To a large degree, the functionality of the H.261 encoder block diagram applies. However, the specifics of quantization and motion estimation/compensation and coding are different.

Recently a second phase of standardization dubbed MPEG-2 has begun. Its aim is efficient coding for up to 10 Mb/s with the further goal of higher-quality results.

SILICON SOLUTIONS. Many digital video applications will require low-cost silicon implementations to become broad-based. Toward the end of 1990, there was a flurry of announcements of chip set solutions for image and video compression. Some are nonstandard approaches; others conform to such draft standards as JPEG and H.261.

Solutions for JPEG were offered first by C-Cube Microsystems Inc., San Jose, Calif., then by LSI Logic Corp., Milpitas, Calif. The former is a single-chip CL550 announced in late 1989 and conforms to an early revision of the JPEG draft. The company is currently reworking the design to meet the latest JPEG specifications. LSI Logic's semicustom two-chip solution combines the L64735 DCT processor with the L64745 quantizer plus JPEG variable-length coder. The partitioning into two chips kept costs down because smaller die have higher yields and can reside in cheaper plastic packages.

The architectural approaches of C-Cube and LSI Logic are similar. Both the CL550 and the LSI parts implement the JPEG algorithm, but the user may change such JPEG parameters as image resolution, number of components, and the quantization and Huffman code tables used.

H.261 products are available from LSI Logic and Graphics Communications America Ltd. (GCA), Glen Ellyn, Ill. LSI Logic announced a seven-chip building block family for general full-motion video encoding and decoding (including H.261) in September 1990, and GCA followed with a 12-chip building block family about a month later. Both are best classified as function-specific video codec building blocks.

The LSI Logic line consists of four processors and three coding and decoding chips. The processors are the L64720 for motion estimation, the DCT L64730, the L64740 for quantization and L64760 for intra/inter-frame decision. The other three chips are the L64715 Bose-Chaudhuri-Hocquenghen (BCH) error-correcting codec, the L64750 H.261 variable-length encoder and L64751 H.261 variable-length decoder, all specific to H.261.

The four processors may be used in any transform-based compression system. For instance, the MPEG video coding loop (minus the variable-length coder) can be built with the LSI chips.

DESIGN FLEXIBILITY. Function-specific building blocks give video system designers the freedom to configure their own compression architecture at a system level. The parts do not require complicated microcode and are generally easy to use.

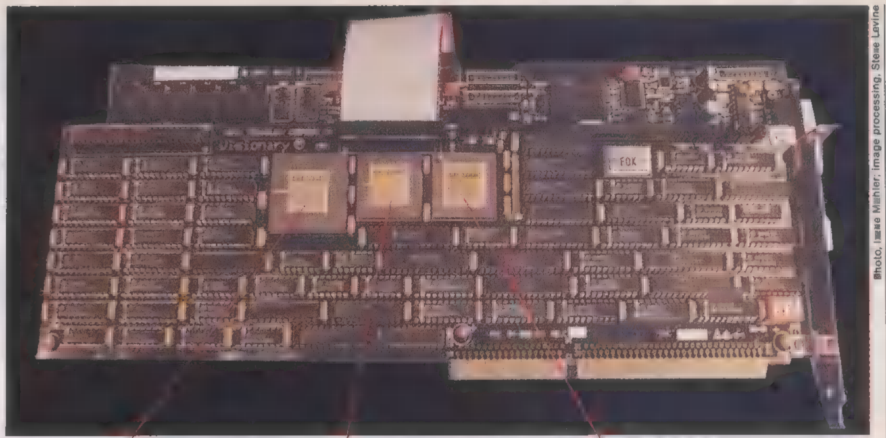


Image compression boards that comply with the Joint Photographic Experts Group (JPEG) proposed standard are becoming available. The one shown here—Visionary JPEG Compression Engine from Rapid Technology Corp., Amherst, N.Y.—has three LSI Logic Corp. ICs performing raster-to-block conversion, the discrete cosine transform, and quantization and coding. Its connection to Rapid Technology's Visionary Video Board (in the back) allows real-time video data or stills to be directly transferred between the two boards.

In the category of proprietary solutions, there is a two-chip set from Intel Corp., Santa Clara, Calif., and a single-chip from UVC, Irvine, Calif. The two-chip Intel i750 comprises a pixel processor and a display processor, both components of Intel's Digital Video Interactive (DVI) architecture. The pixel processor has a 48-bit-wide microcode instruction and supports the compression and decompression of images and motion video. It also synthesizes graphics primitives. The display processor takes bitmaps from memory and displays them on the CRT. Since May 1990, Intel has been shipping a software product using the chips to perform compression and decompression based on a vector-quantization algorithm achieving real-time performance for 256-by-240-pixel images. A feature of Intel's approach is its programmability.

In its product announcement, UVC claims a chip capable of real-time 500:1 compression, using purely intra-frame techniques.

One other company, SGS-Thomson Microelectronics, Phoenix, Ariz., has announced parts suitable for use in a compression system. It has several DCT processors (STV3200, STV3208, and A121) and a motion estimation processor (STV3220).

A DIGITAL TREND. Many new applications in video technology will be digital, as is underscored by the Federal Communications Commission's recent statement that it favors an all-digital HDTV approach. In the computing arena, interest is already growing in the integration of video with graphics and audio. Often referred to as "multimedia" applications, these will be used in interactive education, next-generation graphics systems, network videoconferencing, and other user-friendly systems.

In short, the technology encompassing digital video and audio integrate the worlds of broadcasting and communication with the world of computing. Ten years from now, these three industries will not be distinguishable.

TO PROBE FURTHER. Two textbooks with good discussions of general image encoding techniques are *Digital Image Processing* by William K. Pratt (John Wiley and Sons, New York, 1991) and *Digital Image Processing* by Rafael C. Gonzalez and Paul Wintz (Addison-Wesley, Reading, Mass., 1986). Arch C. Luther wrote an *IEEE Spectrum* article on interactive digital video (DVI) technology in September 1988, and subsequently authored a definitive book on DVI technology entitled *Digital Video in the PC Environment*, 2nd edition (McGraw-Hill, New York, 1990). Another recent book on HDTV is entitled *HDTV: Advanced Television for the 1990s* by K.Blair Benson and Donald G. Fink (McGraw-Hill, New York, 1991).

The April 1991 issue of the *Communications of the Association for Computing Machinery* (CACM) was devoted to emerging compression standards with relevance to digital multimedia.

ABOUT THE AUTHORS. Peng H. Ang (M) joined LSI Logic Corp., Milpitas, Calif., in July 1984. He is vice president and general manager of the digital signal processing (DSP) business unit, which introduced a line of image and video compression ICs in September 1990.

Peter A. Ruetz (M) joined LSI Logic in June 1986. He is currently a senior member of the DSP group's technical staff.

David Auld joined LSI Logic in 1990. He is currently the applications manager of the DSP group. Prior to joining LSI, he was with Inmos Corp., which later became part of SGS-Thomson Microelectronics. ◆

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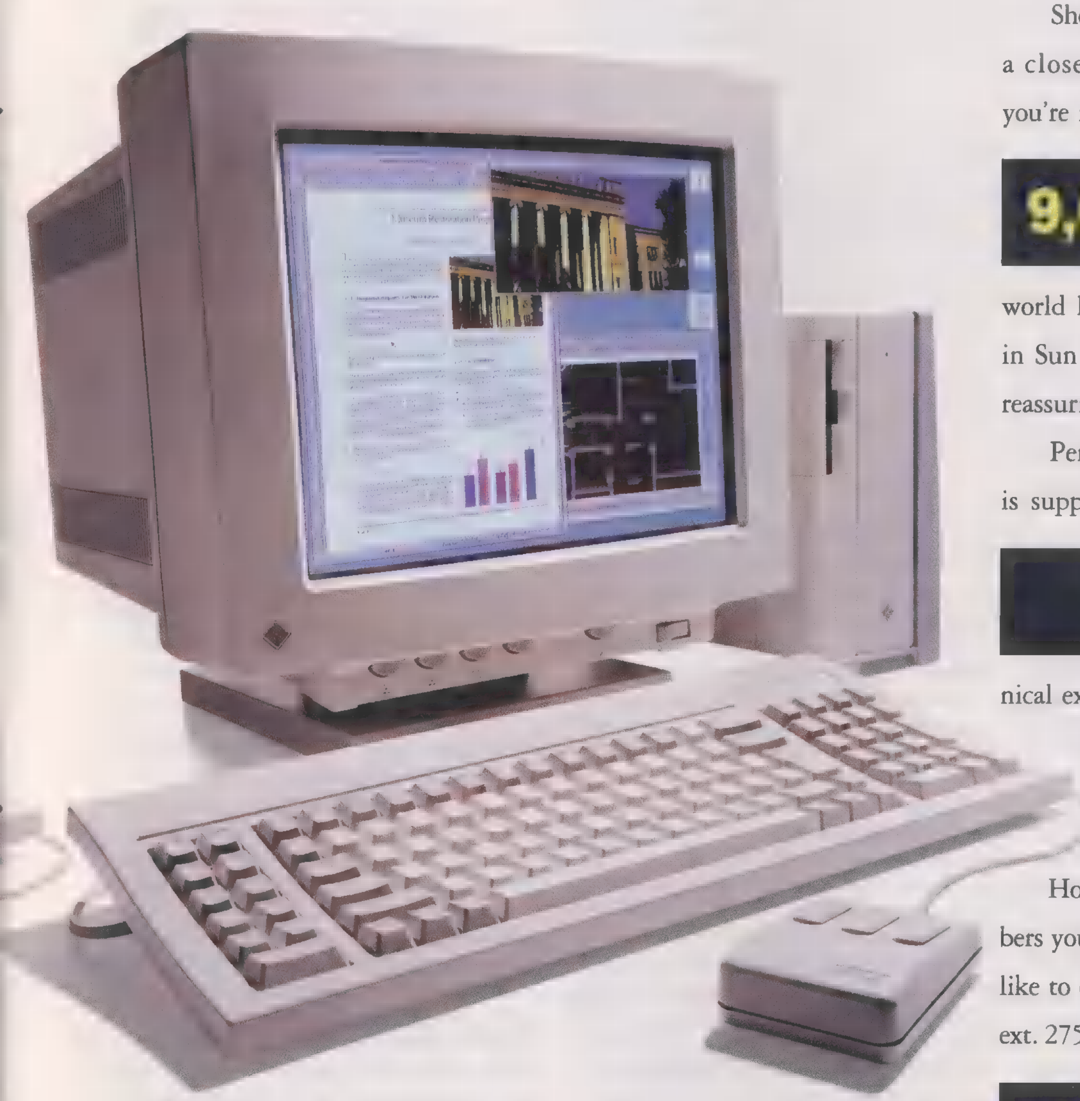

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Teaching information networking

Business and public policy, as well as computers and telecommunications, are studied in a new integrated program at Carnegie Mellon

You have just been assigned the job of starting a new design project. Your first charge is to check the published literature on the subject, so rather than go to the library, you turn to the workstation in your office. Using Boolean search operations, you begin a traditional key word search in scholarly journals to obtain a list of relevant articles. As you display the articles on your workstation, you browse through the journals for other articles that might be helpful.

Finding a journal that publishes extensively in your field, you decide to check the articles in several issues using the "display first page" command. With some of the articles, you want the references listed, so you use the "display last page" command. You also use the "zoom in" and "zoom out" commands to examine the diagrams closely.

This scenario describes an electronic library system of the future, perhaps the near future. Such an electronic system will be part of a world that is coming dramatically closer to being completely interconnected by computer and telecommunications technologies. But designing such systems will require experts in a relatively new and evolving discipline: information networking.

The first master's degree program in information networking was inaugurated in August 1989 at Carnegie Mellon University in Pittsburgh. Under the aegis of the new Information Networking Institute (INI) there, the 14-month program was developed with the support of Bell Communications Research (Bellcore), Livingston, N.J., the research arm of the Bell operating companies in the United States.

Bellcore and the operating companies provided a US $1 million start-up grant so that a trained pool of people would be available to evaluate potential information networking applications and design them for the companies' clients and end-users. According to Bellcore, information networking could bloom into a large and complex area of study much as computer science did in the 1960s.

A FIRST. Carnegie Mellon is not alone in putting together a master's program in information technology. Already master's programs in telecommunications management, information systems engineering, and similar subjects exist at such schools as the Polytechnic Institute of New York, the University of Colorado, the University of Pittsburgh, and George Washington University. But while these programs tend to combine two academic disciplines—for example, telecommunications and management or information systems and management—Carnegie Mellon's program is the first to treat information networking in an agenda that includes graduate-level study in four academic areas: telecommunications, computers, business, and public policy.

The information networking program was the brainchild of Irwin Dorros, Bellcore's executive vice president of technical services. He hopes the progam will not only flourish at Carnegie Mellon, but will be picked up by other universities as well.

"We still have a long way to go to reach the full networking capabilities required by the Information Age," Dorros said. "This new program recognizes that the information technologies have been merging and advancing at an incredible pace. Information networking is the engine that will drive business, industry and, indeed, our society in the years to come."

How that engine will be fueled will require a combination of processing, delivering, and managing information across both public and private networks. But once in place, information networking will enable end-users to retrieve information easily from distributed sources, carry out a variety of transactions, and communicate interactively in multiple media—voice, data, text, image, and video. Designing such systems, however, will require knowledge of such diverse areas as distributed computing, high-speed networking, protocol analysis, and multimedia displays.

The Information Networking Institute is a joint venture of three Carnegie Mellon schools: the Carnegie Institute of Technology (the engineering school), the School of Computer Science, and the Graduate School of Industrial Administration (the business school). Carnegie Mellon faculty retain appointments in their traditional academic departments, where they remain eligible for promotion and tenure.

Carnegie Mellon professor Marvin Sirbu, who was largely responsible for developing the institute's program, recalled that it immediately attracted a great deal of university support. "[Information networking] was a natural extension and enlargement of research and intellectual ideas that already existed at the university," he said.

Students entering the program hold a recent bachelor's degree in electrical engineering, computer science, or a closely related field. The curriculum is divided into two parts. The first part consists of required and elective courses taken in two and a half semesters (a total of 35 weeks) while the second is a 14-week period devoted to a design or research project [see table].

Typical technology courses include such traditional electrical engineering ones as communications engineering and computer architecture, plus courses like circuit and

Alex Hills University of Alaska

Carnegie Mellon master's program in information networking

Fall semester[1]		Spring semester		Summer semester		Fall semester
Circuit and packet switching Network algorithms Introduction to business Elective	Circuit and packet switching Database management Introduction to business Elective	Communications requirement[2] Distributed systems Computer architecture requirement[2] Tehnical elective	Communications requirement Distributed systems Computer architecture requirement Technical elective	Corporate telecom. networks IS development Managing IS Information network implementation Project seminar	Final project or Thesis research	Continuation of final project or Thesis research Telecommunications and information policy environment

1 Each half-semester is seven weeks long. 2 Course depends on student's background. IS = Information systems.

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packet switching developed specifically for the program and computer science courses in operating systems and distributed systems.

Business principles are covered in an introductory course developed for students with the technical backgrounds of the master's candidates. Other business courses focus on management information systems, corporate telecommunications networks, and systems design and implementation—courses that show how businesses use and process information and how to identify information networking opportunities.

The program also covers telecommunications and information regulation by government, as well as the use of information networking as an element of competitive strategy. Students may also choose from a broad range of electives, including software engineering, artificial intelligence, and the impact of information technology on society.

GROUP PROJECTS. Students integrate what they have learned in either a final project or a research thesis. Most participate in a single intensive group design project where they apply their information networking knowledge to a typical real-world problem.

Students electing to write a thesis work by themselves. Their research is generally focused on such information networking topics as communications, computer hardware and software, and applications.

The previously described electronic library system for scholarly journals was a final group project. In examining the business and technical possibilities of such a system, the students considered such relatively recent developments as large-screen workstations, high-speed networks, and large-capacity storage devices—all critical to a wide array of information networking systems. They then investigated the general architecture for the system; the specification of logical entities and their relationships; mechanisms for transport and storage of documents; a user interface; security aspects; and billing fees and arrangements.

Marketing and legal issues were examined as well, and students developed a business plan with budgets and schedules for implementing the system. Implementation risks were also considered along with contingency plans for dealing with them.

BELL PROGRAM. Another program run by the Information Networking Institute is a slimmed-down version of the master's program—a 14-week course called the Advanced Technology Innovation (ATI) program. Offered only to employees of Bellcore and the Bell operating companies, the non-degree program is given twice a year on the Carnegie Mellon campus. Students selected by their organizations—65 graduated in 1990, and a similar number is attending in 1991—are generally in mid-career with some years of experience. Courses are less theoretical and conducted on a more practical level than those in the master's program.

The ATI program first focuses on the study of how companies use information technology. It then reviews information networking principles to indicate how network technologies can be used in business situations. In particular, ATI emphasizes how a competitive advantage can be gained by using information technology. Where possible, case studies are used to add realism.

The goal is to give ATI students an understanding of emerging information and network technologies and show how those technologies can be applied to business needs. The program is taught by Carnegie Mellon faculty and staff, researchers from Bellcore and the operating companies, as well as other lecturers.

CENTER FOR RESEARCH. The Information Networking Institute is also a center for research that reflects the institute's interdisciplinary perspective. Bellcore supports many projects undertaken by Carnegie Mellon faculty from various departments. Among the topics being researched are methods of resolving inconsistency in distributed file systems, the operational and organizational implications of electronic document interchange systems, and the future of broadband service to the home.

In one project, for example, switching networks for distributed real-time systems, the focus is the viability of packet-switching networks in situations where shared-media, local-area networks are commonly used. The application currently being considered is a large, highly automated factory, with a network carrying a mix of voice, image, and control information.

Of particular interest in this project is the timely delivery of messages, with timeliness critical for some messages but not for others. Algorithms are being developed to guarantee that certain classes of messages will be delivered within set time constraints.

Initiatives like the Information Networking Institute raise issues about the proper relationship between industry and academia. The master's program in information networking and the ATI program were created in response to a request and with aid from Bellcore. But Carnegie Mellon determines and controls the content of the master's program curriculum, and the program is available to anyone meeting admission requirements. The non-degree ATI program, on the other hand, was developed to meet the needs of the companies. Accordingly, Bellcore and Carnegie Mellon jointly determine the content of the curriculum.

TO PROBE FURTHER. Information on electronic library systems and a full description of Carnegie Mellon University's graduate students' work on this subject can be found in "Development plan for an electronic library system," an Information Networking Institute technical report. Contact: Information Networking Institute, Carnegie Mellon University, Pittsburgh, Pa. 15213.

The strategic use of information technology is treated in *Competing in Time: Using Telecommunications for Strategic Advantage* by Peter G.W. Keen (Ballinger, 1986). David A. Runge discusses the same subject in *Winning with Telecommunications: An Approach for Corporate Strategists* (International Center for Information Technologies, 1988).

ABOUT THE AUTHOR. Alex Hills (SM) was the first director of Carnegie Mellon's Information Networking Institute in Pittsburgh. Aside from the time he spent there, he has lived in Alaska for over 20 years, working at jobs ranging from commercial fisherman to radio disk jockey to electrical engineering professor. He was extensively involved in building Alaska's rural telecommunications network and is currently director of telecommunications at the University of Alaska in Fairbanks. ◆

Information networking: the graduates' view

Judging by its graduates' reactions, the 14-week advanced technology innovation (ATI) part of Carnegie Mellon's information networking program hit a responsive chord. They almost immediately formed an alumni association, which held its first annual meeting last April in Washington, D.C.—a speedy response to a program launched only in the fall of 1989. Master's program graduates have also joined the group. The second annual meeting is planned for next April in California.

"We're setting up an annual refresher conference so people can stay current in the discipline," explained Quentin Hovland, this year's alumni chairman and an area manager for technology planning at Southwestern Bell Telephone Co., St. Louis. A Bell System veteran of 20 years, the last five with Southwestern, Hovland is also a spring 1990 graduate of the ATI program, which by last summer had about 120 graduates. He termed the program "an excellent experience. It gave me a broad perspective on technology and how it can be applied, which is critical to our future planning."

In his job, Hovland is responsible for developing "from concept to deployment a new way to deliver services. It means making changes in just about every part of the company." The ATI course familiarized him with the various aspects of service creation, he continued. "The phone companies have been pretty good at producing specialists; [the ATI program] produces generalists."

Also pleased with the ATI program is Tom Appleby, manager of strategic planning for technology and services at BellSouth, Birmingham, Ala., where he has worked for 18 years. "It combines telecommunications with computers and business strategy like no other program," he said.

Just as impressed with information networking as a discipline is Paul Zimmerman, who is on the technical staff of Bellcore's Network Transport Requirements Division, Red Bank, N.J. He was in the first master's program, receiving a degree in December 1990 that complemented his 1988 Penn State BEE. "The traditional EE master's program is too narrowly focused, and I wouldn't have had computer science or business courses," he said.

—Alfred Rosenblatt

Optical lithography stalls X-rays

Ultraviolet light will prove good enough for the quarter-micrometer geometries of even 256M-bit memory chips

Optical lithography for IC fabrication, only a few years ago thought to be on its last legs, has now found rejuvenation. To the surprise of many engineers who believed the forming of such small features was possible only with electron-beam or X-ray lithography, optical lithography is being used to make advanced IC chips, with 0.35-micrometer geometries in research, 0.5 μm in production.

What has encouraged this revival in optical lithography has been continuing advances in photoresists, phase-shifting masks, high-numerical-aperture step-and-repeat optical systems, multilevel-resist processing, and top-surface imaging techniques. In fact, the advances have been so numerous that it now appears that X-ray lithography—and its huge capital investment—may not be needed until the next century.

With the drive to manufacture ever more complex chips, the minimum feature size of ICs has been steadily shrinking to below 1 μm. The test bed for the smaller geometries is the dynamic random-access memory (DRAM) IC.

Unlike the more complicated chips—such as application-specific ICs (ASICs), microprocessors, and logic ICs—DRAMs incorporate many repeating cell structures. Because that structure makes DRAMs easier to design and manufacture, advances in IC processing are first tried out in DRAM manufacturing before they are used to produce more complex chips. With mass-produced 64M-bit DRAMs now on the horizon, the need to fabricate 0.35-μm feature sizes becomes critical. The key lithography issues for DRAMs are resolution, image field size, level-to-level alignment, wafer size, and photomasks.

To develop a perspective on DRAM lithography needs today, the Soft X-Ray Lithography Workshop held last January at the Lawrence Laboratory, Berkeley, Calif., drew on information from industry, academia, and government. Workshop participants found that optical lithography will be sufficient for the next few generations of DRAMs, and that X-ray lithography will not be needed until about the year 2000, when 1G-bit DRAMs will make their appearance [Table 1]. This prediction is from an industry group that could be regarded as advocates of X-ray lithography.

Gary E. Flores and Bruce Kirkpatrick
KTI Chemicals Inc.

Historically, DRAM cell density (cells per square centimeter) has increased by a factor of 3 for each new generation, which occurs nearly every three years, with lithography accounting for two-thirds of the increase and semiconductor technology for one-third. Further, each generation has experienced a fourfold increase in bits per chip. Both the increase in chip area with each generation and the reduction in minimum design rules present serious challenges for the lithographer. Enlarging the chip area increases the probability of incurring chip defects, thus limiting manufacturing yield. The industry's demand for smaller design rules means higher precision in feature size control, which explains why photoresist and lithography equipment suppliers continually strive to improve resolution.

X-ray lithography won't be needed until gigabit, 0.15-μm DRAMs arrive

A challenge for optical stepper manufacturers is the need to simultaneously enlarge field size and increase resolution, both of which are tightly coupled in lens design and manufacturing. These needs require careful attention to various lens residual aberrations such as spherical aberration, coma, astigmatism, field curvature, and distortion—all of which will limit both the field size and resolution.

For example, lens distortion is one of the prime factors affecting lens performance, and enlarging the lens image field size requires a distortion correction in proportion to the cube of the image field. This involves eliminating all possible distortion in both design and manufacture. By intentionally lowering design tolerances for aberration components and minimizing manufacturing imperfections of lens defects, optical lithography stepper suppliers have been able to meet the demands of the IC industry.

UV DOMINATES. Of all lithography techniques, optical lithography based on ultraviolet (UV) light in the 200–400-nanometer range continues to be the predominant system for IC manufacturing technology [see Table 2 for basic characteristics of optical and nonoptical techniques]. The ultimate resolution potential of optical lithography appears to be near 200 nm.

Near-UV technology, which includes broadband, g-line (436-nm), and i-line (365-nm) imaging, continues to dominate because of the maturity of both its optical components and its photoresist chemistry. Several types of near-UV projection printing systems are commercially available and in production. These include 1× step-and-repeat and 1× scanning systems, both using reflective lens elements and broadband exposure sources.

Supplanting them are 5× stepping reduction systems based on refractive optic elements and monochromatic exposure sources. Because the 1× systems have fewer lens elements and benefit from symmetry, they have smaller asymmetric lens distortions and aberrations than their 5× counterparts. They also have larger image field sizes.

However, the 1× scanning systems have fallen out of favor for more advanced technologies because of the difficulty of manufacturing submicrometer 1× masks. (With 5× reduction masks, errors in feature size and defects are reduced by a factor of 5 during pattern transfer to the wafer.) Furthermore, 1× scanners have insufficient depth of focus across large wafers, and so require steppers. But they are used quite commonly in combination with reduction systems for those masks whose minimum features are 1 μm or larger.

LESS URGENCY. Deep-UV lithography is not yet accepted for production processes for several reasons. Most important is the lack of commercially available positive- and negative-tone photoresist systems for deep-UV wavelengths. (Deep-UV lithography needs both positive and negative.) In addition,

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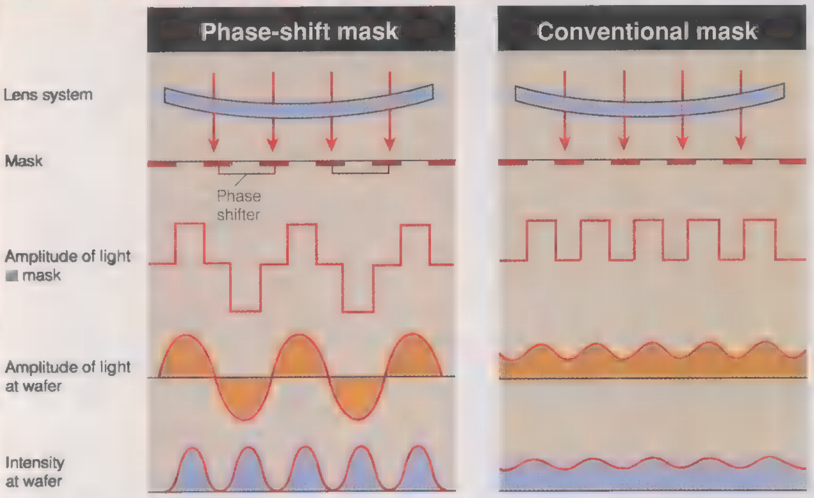
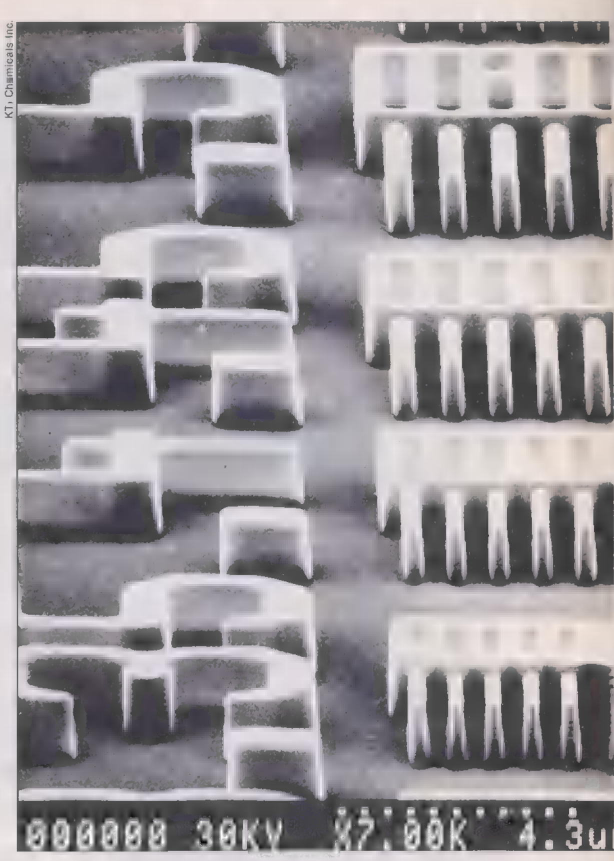
Optical phase-shifting lithography



[1] In a basic form of phase shifting, every other element in a closely packed mask contains a phase shifter—an extra patterned layer having a high refractive index. By shifting the phase of the light passing through it, the shifter creates interference. As a result, the light amplitude at the mask varies from 1 to 0 to –1, whereas it varies only from 1 to 0 at a conventional mask. This greater variation at the phase-shifted wafer provides a considerably wider range of both intensity and amplitude. The intensity, which is proportional to the square of the amplitude, restores the spatial frequency of the mask openings, but with far greater contrast and, therefore, resolution.



[2] From top to bottom, lines and spaces in right-hand structures are 50, 45, 40, and 35 μm wide. The pattern in silicon was made with an ASM i-line stepper and KTI Chemicals i-line photoresist.

negative-tone resists are temperature-sensitive and therefore hard to handle in a manufacturing environment. Also, extensive gas-handling facilities are required for deep-UV excimer laser sources, and optical components have to be replaced often because the intense laser energy devitrifies lenses quickly. Fortunately for process managers, the recent advances in i-line technology make acceptance of deep-UV lithography less urgent.

The key parameters in lithography are minimum resolvable feature size and the depth of focus. Both are related to the wavelength of light and the lens's numerical aperture (NA) by the Rayleigh criteria. According to the criteria, the size of the minimum resolvable feature varies directly with the wavelength and inversely with NA, with a constant of proportionality of k_1. Depth of focus also varies directly with wavelength but inversely with the square of NA, with a constant of proportionality of k_2

The constants are functions of the photoresist, the stepper lens, and the substrate. Until recently, k_1 values of about 1 were common in production processing. With new photoresist systems, however, values are about 0.8 for production and 0.48 for controlled laboratory processing. For an optical system at its diffraction limit, k_2 is 0.5.

For a given resolution, the optical system using the shorter wavelength will have the largest depth of focus. That is why i-line technology, with its shorter wavelength than g-line, has gained such attention over the past two years. Adequate depth of focus is essential for maintaining tight process control, especially when stepper repeatability and wafer topography are an issue. Just as a snapshot camera is hard to focus on two objects at different distances, the photolithographic process finds it difficult to focus simultaneously on the peaks and valleys of the IC wafer below it.

Previously, i-line lithography was thought to be a transition technology between the workhorse g-line technique and the newcomer, deep-UV lithography. Now, with the rapid availability of optics having high transmittance and tight tolerances of index of refraction for i-line, a new generation of i-line stepper systems has emerged. At the Society of Photo-optical and Instrumentation Engineers (SPIE) Microlithography Symposium last March in San Jose, Calif., several major stepper manufacturers, including Canon U.S.A. Inc., GCA Corp., Nikon Precision Inc., and ASM Lithography Inc., presented test results on new i-line steppers. They had 0.50-μm resolution for manufacturing 16M-bit DRAMs as well as ultimate resolution of 0.35 μm. Such continued improvement in lens optics, in conjunction with fewer lens defects, will provide imaging capability near the diffraction limits of an optical lens.

Optical phase-shifting masks have also shown promise in improving resolution and depth of focus. These shifting masks are two-level mask structures that can improve resolution in optical lithography systems 25 to 100 percent by using interference to cancel diffraction effects. The concept, first introduced by Marc O. Levenson and coworkers at IBM Corp. in 1982, has attracted serious interest over the last year. Initially Levenson proposed an alternating phase-shifting technique, applicable for patterning line and space pairs. Since then, a myriad of other techniques have quickly evolved from this approach to address the various other patterns in IC processing; for example, subresolution, rim, and attenuat-

Defining terms

Excimer laser: a coherent light source based on krypton fluoride, krypton chloride, argon fluoride, and fluorine species.

g-line: the 436-nm wavelength of the UV light spectrum.

i-line: the 365-nm wavelength of the UV light spectrum.

Negative-tone photoresist: a photoresist in which unexposed regions are more soluble than exposed regions.

Novolac resin: a phenolic polymer; the major component of positive-tone photoresists for near UV.

Numerical aperture (NA): the acceptance angle of a lens.

Photoactive component (PAC): the species in a photoresist that is sensitive to incident radiation; for positive photoresists, usually a diazonaphthoquinone.

Positive-tone photoresist: a photoresist in which exposed regions are more soluble than unexposed.

Photoresist: photosensitive polymer films used to transfer patterns in IC manufacturing.

Stepper: a machine that applies patterns on wafers by repeating, or stepping, an image across the wafer's surface.

Lithography without light

Electron-beam lithography, in which electrons trace a pattern in photoresist, can resolve details as small as 0.10 μm. But it is slow (wafer throughput is low) and equipment is expensive. (An electron-beam lithography machine costs about US \$4–\$5 million; an optical lithography machine costs about \$1.6 million.) Electrons also tend to scatter in the photoresist and wafer substrate during patterning—causing what is called the proximity effect, where dense patterns become distorted unless proximity correction techniques are used.

As a production tool, electron-beam lithography is largely limited to fabrication of photomasks and short-run application-specific ICs. Electron flood exposure and electron projection systems now under development at AT&T Co. and Hitachi Ltd. may improve throughput, but as yet they are not commercially available.

Ion-beam lithography has also been pursued as a potential submicrometer lithography system. Because ions are more massive than electrons, they scatter much less and therefore require virtually no proximity corrections, providing inherently better resolution than electron-beam lithography. Unfortunately, ion-beam lithography is used only in R&D work because of the lack of readily available, reliable ion sources and the greater maturity of competitive electron-beam equipment.

X-ray lithography overcomes many of these limitations and offers resolution potential down to 0.02 μm with high throughput. These benefits have made it an attractive approach for achieving submicrometer resolution in a manufacturing environment for future dynamic RAM technologies. Also, since the low energy of soft X-rays (0.4–5 nm) eliminates scattering effects, they require no proximity corrections. Finally, soft X-rays offer low photoresist absorption and a large depth-of-focus latitude, which results in straight-walled profiles in thick films.

Despite the advantages of X-ray lithography, several challenges still hinder its progress. Heading the list are fabrication problems for membrane masks, which, being different from the masks used for optical lithography, are more difficult to pattern and repair. And conventional X-ray tubes are not bright enough for production service; they are now practical only for R&D applications.

Where higher intensity is needed, two new sources of X-rays are plasma and synchrotron radiation. A single synchrotron source can support multiple lithography systems, but its cost and size requirements have been a major barrier for many IC manufacturers. Plasma-based sources are more conventional in size and more cost-effective, but they deliver less power than synchrotron radiation and consequently wafer throughput is marginal. Additionally, plasma-based systems require optical elements with highly perfected reflective properties. For example, lens elements have a tolerance of less than 1 nm over an entire surface, which is several orders of magnitude finer than lens elements used in optical steppers.

The major U.S. efforts for X-ray lithography are at IBM Corp. and AT&T Co., where two different approaches are in place. IBM is committed to 1× proximity X-ray lithography using a synchrotron source, while AT&T is pursuing a projection system with a plasma source.

IBM has already fabricated 0.5-μm CMOS devices with this technology. According to an IBM spokesman at the Berkeley Soft X-ray Lithography Workshop, the company has scheduled full production of 0.25-μm memory devices for 1997. Also participating in the project are Motorola Inc. and Siemens AG. In Japan, consortia reportedly are developing 10 synchrotron lithography systems. Because of the extremely high capital expense and the fabrication space requirements of X-ray lithography, other manufacturers have yet to announce plans in this arena.

—G.F., B.K.

ed phase shifting—and various combinations of these techniques—are being tried.

HIGHER CONTRAST. Phase shifting uses the interference effects of coherent light to form a higher-contrast image on the wafer plane. This produces higher resolution, larger exposure latitude, and greater depth of field [Fig. 1]. Currently several major IC manufacturers are exploring phase-shifting masks and i-line technology for 64M-bit DRAM production. Fujitsu Ltd., Toshiba Corp., and Matsushita Electric Industrial Co. have already announced success with this approach for building fully functional 64M-bit DRAM devices in the laboratory.

Phase-shifting masks can extend i-line technology to the 0.35-μm limit and perhaps beyond for 64M-bit DRAM production. However, this technology requires a new level of mask fabrication technology and the development of new computer-aided design software that can place phase-shifting structures in the circuit pattern design. It will be interesting to see if phase-shift masks serve deep-UV lithography down to 193 nm. If so, they could provide 0.15 μm resolution and hence minimize the need for X-rays. Much more work in this area needs to be, and assuredly will be, done over the next few years.

Optical phase-shifting masks can improve resolution by up to 100 percent

Other opportunities for improving resolution and depth of focus include multilevel resist processing and top-surface imaging. These techniques overcome the effects of substrate topography, substrate reflectivity variations, and depth of focus limitations. They perform pattern transfer where optical imaging occurs, within a thin top surface of the photoresist film. (In contrast, in single-layer positive resists, pattern transfer occurs through the entire depth of the film.)

The top surface then provides a mask for pattern transfer to the underlying photoresist. The effect of thin-film interference within the photoresists is thus suppressed, reducing both depth of focus and exposure latitude. These techniques have a resolution equal to or better than the Rayleigh limit.

Receiving the most attention among these techniques is the contrast enhancement layer (CEL) method, a two-level resist process. A photobleachable film of the CEL material is coated on a conventional photoresist film. Once exposed, the CEL material becomes transparent in the exposed regions and remains opaque in the unexposed regions, forming a contact mask, which enhances contrast.

Although top-surface imaging and multilevel-resist processing have demonstrated some advantages, they have not enjoyed wide use in optical lithography production because of their processing complexity and cost. However, as the frontiers of optical lithography are continually pushed, these techniques will continue to be reexamined and will ultimately provide the benefits needed for extending optical lithography.

Meanwhile, harnessing the full potential of single-layer photoresist processing is still one of the most attractive possibilities. Recent research has led to new single-layer photoresist materials with higher contrast. The greater photoresist contrast means improved resolution, depth of focus, and linewidth control. Higher-contrast resists enhance a weak stepper optical image and produce a more pronounced and better defined photoresist pattern. Improving photoresist contrast is the most cost-effective and manufacturing-worthy method of extending a lithography process.

POSITIVE AND NEGATIVE. Photoresist materials can be classified as either positive or negative tone according to their response to light. A positive-tone photoresist dissolves more readily in solvents in exposed regions than in unexposed regions, while a negative-tone photoresist provides the opposite effect. For years, negative-tone resists represented the main approach in the IC industry. The two major types of negative resists are two-component bisarylazides (cyclized polyisprene) and the one-component copolymer of glycidyl methacrylate and ethyl acrylate (called COP by its developers at AT&T Bell Laboratories). COP is an electron-beam photoresist; its polymers cross-link on exposure to electrons.

However, they suffered from low thermal stability, solvent swelling, and inferior resolution, and they presented an environmental hazard because of the base solvents

they needed. These deficiencies are largely avoided in the two-component positive photoresist systems currently in use for most near-UV optical lithography. Positive photoresist formulations are based on a novolac resin and a diazonaphthoquinone photoactive compound (PAC) dissolved in an organic solvent.

The performance of novolac resists has been enhanced by changes in the molecular weight and structure of the resin and in the PAC molecular structure. These innovations, plus more accurate modeling of photoresist chemistry, have enabled major photoresist suppliers to introduce vastly improved new materials.

KTI Chemicals Inc., Sunnyvale, Calif., uses capped novolacs, in which the PAC is chemically bonded to the novolac resin. This practice adjusts the solubility of the photoresist and counters the tendency of latent images to decay when an exposed pattern is not quickly developed. Other agents are used to give photoresists greater sensitivity and contrast.

The newest generation of photoresists is specifically optimized for i-line lithography. These photoresists give manufacturers wide latitude in choosing exposure and focus, accommodating variations in lithographic equipment. Being heat-resistant, they can withstand the high temperatures of dry etching and ion implantation. Since they are also more sensitive, they require less exposure energy so that wafers can be processed faster for greater throughput. With advanced i-line equipment, their resolution is so improved that new photoresists yield lines 0.5 μm wide or less [Fig. 2].

All trends indicate a strong bull market for i-line lithography for at least the next four years. According to a 1990 survey, U.S. domestic consumption of broadband and g-line photoresists has begun to shrink, while that for i-line photoresist has started a speedy, steady growth.

In comparison, consumption of the newer photoresists for X-ray and deep UV are almost microscopic. From 1991 to 1996, i-line steppers will account for the bulk of stepper purchases, with a peak in the 1994–95 period [Fig. 3]. A similar surge in deep-UV steppers should then occur with a peak in 1998 to meet lithography requirements for the 256M-bit DRAM, bridging the gap between i-line and X-ray lithography.

Clearly the emergence of i-line lithography, with its improved resolution capabilities and depth of focus, will let IC manufacturers postpone the expense of retooling for deep UV and X-ray—a daunting expense when one considers IBM's US $1 billion investment in developing synchrotron X-ray lithography. Until problems with making both X-ray and deep-UV production systems viable are finally resolved, i-line will remain entrenched.

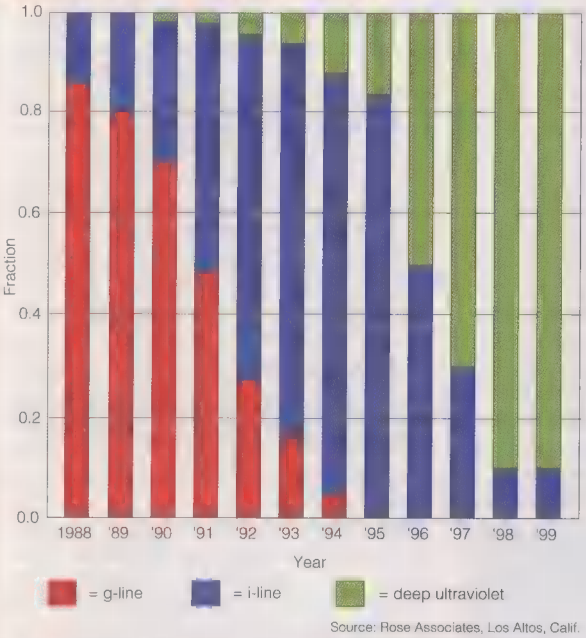
1. Lithographies for dynamic RAM production

Dynamic RAM chip	Design rule, micrometers	Initial production	Peak production	Lithography system
1M-bit	1.00–1.20	1989	1991	G-line stepper
4M-bit	0.65–0.80	1990	1993	I- and g-line stepper
16M-bit	0.50–0.60	1991	1994	I-line stepper
64M-bit	0.35–0.45	1992	1995	I-line/deep-ultraviolet stepper
256M-bit	0.25	1995	1997	Deep-UV stepper
1-G bit	0.15	1997	2002	Soft X-ray proximity and projection

2. Submicrometer lithography characteristics

System	Source	Wavelength/energy	Resolution, micrometers
Electron beam	Electrons	1–5 keV	<0.10
Ion beam	Positive silicon ions	100 keV	<0.10
X-ray proximity and projection	X-ray	0.4–5.0 nm	0.01
Optical projection	Ultraviolet Near-UV —g-line —i-line Mid-UV Deep-UV	200–400 nm 350–450 nm 436 nm 365 nm 290–350 nm 200–290 nm	0.20

Submicrometer optical steppers



[3] Past and future purchases of steppers for submicrometer ICs show a peak for i-line machines in 1994–95. Deep-ultraviolet machines will not become a major factor until about 1996, according to predictions.

ABOUT THE AUTHORS. Gary E. Flores is a senior technical development engineer at KTI Chemicals Inc., Sunnyvale, Calif. His current interests include submicrometer optical lithography and statistical methods for experiment design. He has B.S. and M.S. degrees in chemical engineering from the University of California at Berkeley and Santa Barbara, respectively.

Bruce Kirkpatrick is national marketing manager for KTI. He is a 10-year marketing and sales veteran in the semiconductor materials and equipment industry. He has a B.S. degree in political science from Wittenberg University, Springfield, Ohio.

TO PROBE FURTHER. Burn J. Lin describes phase-shifting techniques in "Phase-Shifting and Other Challenges in Optical Mask Technology" in *Bacus News*, February 1991. The *News*, published monthly, contains papers and news on IC lithography. Bacus is a technical subgroup of the Society of Photo-optical and Instrumentation Engineers (SPIE), and holds monthly meetings on lithographic topics. For information, contact Scott Landstrom, DuPont Photomasks, 2235 Zanker Rd., San Jose, Calif.

KTI Chemicals sponsors an annual Microlithography Seminar, to be held this year Oct. 13–15 in San Jose. Contact KTI, 1170 Sonora Court, Sunnyvale, Calif.; 408-733-3500.

SPIE sponsors an annual Microlithography Symposium; for information, contact SPIE, Box 10, Bellingham, Wash. 98227-0010; 206-676-3290.

Brian Santo reported on progress in "X-ray lithography: the best is yet to come," *IEEE Spectrum*, February 1989, pp. 48–49.

For a textbook on IC lithography, see *Introduction to Microlithography*, American Chemical Society (1983). Contact: American Chemical Society, 1155 16th St., N.W., Washington, D.C. 20036; 202-872-4600.◆

Magnetism without magnets

From Volta's battery there flowed a continuous current of electricity that was soon shown to generate a magnetic field

Modern power and communications systems are designed according to laws governing forces between electric charges and magnetic poles. Some were discovered as early as the 17th century. Others were revealed by scientists in the 18th and 19th centuries. Without those laws, electrical engineering as we know it today would not exist.

The earliest researchers rubbed fur on amber or glass rods to make them attract bits of straw or paper. Magnetic forces were small, and experimenters confused the sources of electricity and magnetism. Rumors circulated that magnetic power was lost when the amber or glass rods were rubbed with garlic and regained when they were smeared with goat's blood. In 1600, William Gilbert, a physician to England's first Queen Elizabeth, cleared up much of the confusion in his book, *de Magnete*, in which he described his work on magnets.

In Germany around 1641, Otto von Guericke cast a sphere of sulphur and charged it by rubbing it with his bare hands while it was rotating. It would then attract pieces of lint or straw. In the most popular theory of the day, electricity was a fluid with properties that let it penetrate solids.

Charles Dufay in Paris in 1733 inferred the existence of two kinds of electricity—vitreous (from glass and silk) and resinous (from charged amber and wool).

These early studies had only static charges to work with, such as could be stored in a condenser or Leyden jar—a glass bottle coated inside and out with a metallic film. The inner electrode was charged by successive applications of a rubbed glass or resinous rod.

Despite this handicap, Charles Coulomb, in 1785, stated a quantitative law of electricity, the first ever enunciated. He verified that the force of either attraction or repulsion between two small charged spheres is inversely proportional to the square of the distance between them.

John D. Ryder

But it was not until 1800, when Alessandro Volta in Italy announced the primary electric battery, that continuous electric current could be made to flow at an experimenter's will. Basic to Volta's "pile" were two thin disks of a pair of metals separated by a damp pad. He found zinc and silver to work best when separated by a disk of cardboard moistened in brine. Layers of this sandwich made up the pile.

Volta's invention of the battery opened up a whole new field for study. Humphrey Davy, in England, for one, used current from a voltaic pile in 1807 to isolate sodium and potassium by electrolysis.

In parallel with these discoveries experimenters were speculating that electricity and magnetism were related. The evidence in favor of a relationship kept mounting. Both electric and magnetic forces exhibited powers of attraction and repulsion, both had positive and negative modes and north and south poles, steel needles were magnetized by nearby lightning strikes, and Benjamin Franklin in 1752 had shown that lightning was electrical in nature. But the precise nature of the link between electricity and magnetism remained unknown.

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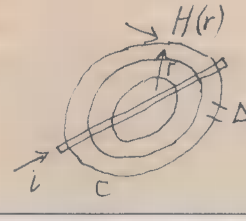

$$\oint_C H \bullet dl = i$$

The availability of continuous current from Volta's pile set off further studies of the link in Europe. Hans Christian Oersted, a professor of natural philosophy (physics) at the University of Copenhagen, when lecturing in 1819, passed a current through a wire lying on top of a compass. As the current started to flow, he noticed that the needle of the compass moved. When the current ceased, the needle returned to its original position. The effect was found to be circular around the wire.

The Dane experimented for several months and in 1820 sent a paper to major journals in Europe, announcing he had observed the generation of a magnetic field by a current. His finding set off a frenzy of activity aimed at applying the action.

The news of Oersted's discovery reached Paris in September 1820, astounding a meeting of the Académie Royale des Sciences. Many members refused to believe the announcement—but not André Marie Ampère.

Ampère picked up and ran with Oersted's new theories and within two weeks showed that the deflection of the magnetic needle could be predicted by what today is called the right-hand rule. He also observed that a coil of wire carrying a current developed magnetic poles and acted as a bar magnet without the presence of iron. This device he called a solenoid.

Ampère soon became the leader of electrodynamics, the name he coined for the newly discovered phenomena. His was the first experiment in magnetism to be performed without a magnet, and his work made electrodynamics a precise and mathematical subject. The current-field relationship is known as Ampère's law and is given in its original form (courtesy of the Burndy Library, Norwalk, Conn.) and in modern notation in the illustration. In the modern version, H is the magnetic field in amperes per meter, dl is a vector element of distance, C is the integration contour, and i is the current passing through the area bounded by C. Magnetic fields encircle currents.

TO PROBE FURTHER. A few of the many books giving further background on the developments described in this article are: R.S. Kirby et al., *Engineering in History* (McGraw-Hill Book Co., New York, 1956) (now in Dover paperback); R.A.R. Tricker, *Early Electrodynamics: The First Law of Circulation* (Pergamon Press, New York, 1965); and *Dictionary of Scientific Biography*, edited by C.C. Gillispie (Scribner's, New York, 1970). Ampère's own paper appears in the sixth volume of the *Mémories de l'Académie Royale des Sciences de l'Institut de France* (Firmin Didot, Paris, 1827).

ABOUT THE AUTHOR. John D. Ryder (F), former dean of engineering, Michigan State University, East Lansing, and now retired, lives in Ocala, Fla. He was the Institute of Radio Engineers' president in 1955, its editor in 1958 and 1959, and IEEE executive vice president in 1974. His latest book, written with Donald G. Fink, is *Engineers and Electrons* (IEEE Press, 1984). ◆

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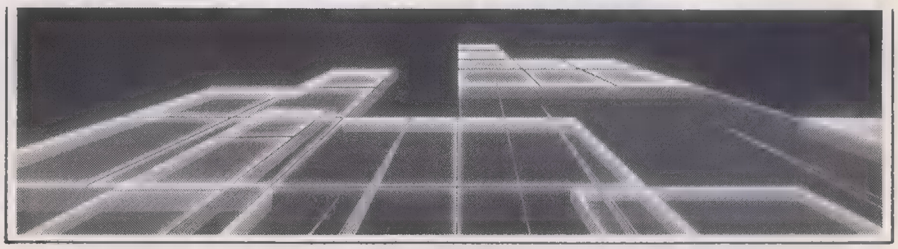

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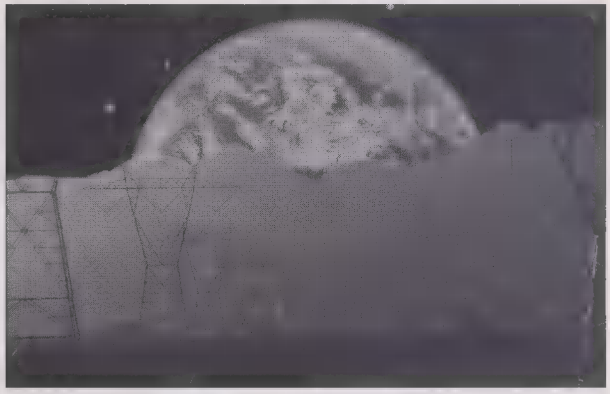

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sent to: Dr. Yacov Shamash, Professor and Director; School of Electrical Engineering and Computer Science; Washington State University; Pullman, WA 99164-2752; (509) 335-8148. Applications should include [redacted] complete professional vita and a list of references. Final screening will begin November 15, 1991 and will continue until the position is filled. WSU is an EO/AA educator and employer. Protected group members are encouraged to apply.

University of California, Santa Barbara, Electrical and Computer Engineering. Applications are invited for at least two tenure-track assistant professor faculty positions, available effective 7/1/92. One position is in the area of optical computing and interconnections, optical communications and networks, or quantum electronics. The other position is in the area of networking and communications. Normally, completion of [redacted] doctorate is required at the time of the appointment. Candidates should have an established research reputation or outstanding research potential, the ability to attract external research funding, and [redacted] strong commitment to teaching at the undergraduate and graduate levels. Applicants should send their resumes and the names and addresses of at least four professional references to: Faculty Search Committee, Department of Electrical and Computer Engineering, University of California, Santa Santa Barbara, CA 93106-9560. Applications will be received until the positions are filled. Proof of U.S. Citizenship or eligibility for U.S. employment will be required prior to employment (Immigration Reform and Control Act of 1986). UCSB is an Equal Opportunity/Affirmative Action employer.

Electrical Engineering. Faculty Opening. Louisiana Tech University. Applicants with an earned doctorate will be judged on effective teaching, ability to improve the growing graduate program, and potential for initiating funded research. Particular emphasis will be given to the [redacted] of VLSI and related technology. Louisiana Tech is developing an Institute for Micromanufacturing which will have state-of-the-art equipment in the microfabrication area. All applications will be considered at the first of each month, starting December 1, 1991, until the position is filled or until final cutoff on May 31, 1992. Send resume indicating visa status and three references to: EE Search, College of Engineering, Louisiana Tech University, Ruston, LA 71272. Louisiana Tech University is an Equal Education and Employment Institution.

Research Position in Applied Science, University of California, San Diego. The Marine Physical Laboratory, Scripps Institution of Oceanography invites applications from scientist for appointments at the Postgraduate Research level. Applicants with an interest in conducting innovative experimental work at sea will be given strongest consideration. Fields of interest include, but are not limited to, sonar or ocean acoustics, geology, geophysics, physical oceanography, autonomous or tethered submersible vehicles, radar oceanography, and marine micrometeorology. Applicants should have [redacted] Ph.D. Applicants will be expected to have [redacted] publication list appropriate to their experience. Salary will be commensurate with experience and qualifications and based on UC pay scale. Immigration status of non- US citizens and names and addresses of three reference should be included with resume. There is the possibility that more than one appointment can be made. Closing date for applications is 31 October 1991. Direct inquiries to Kenneth M. Watson, Director, Marine Physical Laboratory, Scripps Institution of Oceanography, San Diego, CA 92152-6400, (619) 543-1803. The University of California, San Diego is an equal opportunity/affirmative action employer.

Naval Postgraduate School, Faculty Positions. Department of Aeronautics and Astronautics seeks applications for a Tenure Track position in the following area: Avionics (Intermediate or Senior faculty level)—Applicants for the Avionics position should have experience (either industrial or academic) in the development of avionic related items, be knowledgable in digital control, familiar with the integration of aerodynamic, propulsion and navigation concepts, and be willing to develop [redacted] graduate level avionics laboratory. U.S. citizenship is required. Candidate must have Ph.D. in aerospace or related fields, demonstrated research and teaching ability and will be required to teach and perform research at the graduate level. Good communication skills, both oral and written, are essential. In addition to 16 tenure track and 5 adjunct faculty, the department has 15 support staff and offers both M.S. and Ph.D. degrees. Applications will be reviewed beginning November 1, 1991 and will be accepted until the position is filled. Please send resume and names of three references to: Dr. D.J. Collins, Chairman, Department of Aeronautics and Astronautics, Naval Postgraduate School, Monterey, CA 93943, (408) 646-2311. The Naval Postgraduate School is an Equal Opportunity/Affirmative Action Employer.

Electrical Engineering: Cleveland State University, Department of Electrical Engineering, Faculty Position. Cleveland State University is seeking applications for a tenure track faculty position in Electrical Engineering. Appointment will be at the Assistant or Associate Professor level with a competitive salary and rank commensurate with qualifications. Qualifications include a Ph.D. degree, the abilities to teach in B.S., M.S. and Doctoral-level programs and to engage in [redacted] vigorous research program. A specialty in the areas of communications is required. Primary departmental interests in communications includes information theory, coding, modulation and equalization. Knowledge of satellite communication systems and/or practical experience is desirable but not required. Faculty members in the department have the possibility of obtaining research support locally through NASA Lewis Research Center. Deadline: When position is filled, with ongoing screening of applications. Starting date: September 14, 1992. Send resume and list of three references to: Dr. James H. Burghart, Chairman, Electrical Engineering Dept., Cleveland State University, E. 24th & Euclid Ave., Cleveland, OH 44115. Equal Opportunity Employer, m/f/h.

Arizona State University seeks Scien-

RADAR SYSTEMS ENGINEER

Microwave Remote Sensing of the Ocean

The Applied Physics Laboratory of The Johns Hopkins University (APL) continues to pioneer in developing spacecraft and spacecraft radars for monitoring ocean mesoscale activity, climate variations, global ocean circulation, ship routing, deep water oil operations and ocean wave spectra. Our design team is looking for an innovative systems engineer with [redacted] PhD in physics or engineering, or equivalent, to work on the edge of advanced remote sensing technologies. A combination of analytical and hands-on hardware expertise with EM/ocean interactions, propagation, antennas, MMIC RF hardware, Electro-Optics, and digital processing is desired. In addition, the ideal candidate will have ten or more years of relevant experience in radar systems design and development, demonstrated abilities to define and articulate concepts and requirements for novel radar systems and a strong desire for [redacted] leadership position in radar systems engineering.

APL is a nationally recognized research and development organization located midway between Baltimore, MD and Washington, DC on [redacted] 360-acre campus-like setting. We offer a salary commensurate with your qualifications and experience, [redacted] comprehensive flexible benefits package, and an attractive retirement program. If you meet our requirements and are interested in this opportunity, please submit a resume and cover letter which details your education, experience and salary history to:

Recruitment Office
Department LER-722
The Johns Hopkins University
APPLIED PHYSICS LABORATORY
Johns Hopkins Road
Laurel, MD 20723

EOE, M/F/H/V. U.S. Citizenship Required

The Johns Hopkins University

Applied Physics Laboratory

APL

tist/Engineer to manage the staff and operations of the research laboratories of the Center for Solid State Electronic Research. The Center is a shared resource research center in the College of Engineering at Arizona State University. Laboratories in the Center include a 4000 sq. ft. clean room, semiconductor processing equipment, MBE laboratory, optical characterization and electrical characterization labs, X-ray topography, SEM's, mask making facility, and a computational microelectronics laboratory. Research and teaching opportunities are also available. Requires Ph.D. degree in electrical engineering or physics, with 3 years experience in directly relevant field. Applicant must be directly familiar with semiconductor processing and cleanroom facilities, and have characterization experience. Salary negotiable depending upon experience and qualifications. Application deadline November 15, 1991, or on the 15th monthly until filled. Send resume to Dr. L. Akers, Director, Center for Solid State Electronics Research, Arizona State University, Tempe, AZ 85287-6206. Arizona State University is an equal opportunity, affirmative action employer.

The Department of Electrical Engineering at the University of Utah is seeking applications for one or more tenure-track faculty positions. Applicants must have an earned doctorate or must expect to complete a doctoral program by September 1992. Duties of the successful candidate will include undergraduate and graduate teaching and development of a research program. The department has successful and well-funded research programs in electromagnetics, optics, microwave tube design, biomedical engineering, communications, signal processing, and microelectronic materials and devices; we will entertain applications from candidates in any of these areas. We expect to make the appointment at the Assistant Professor level, but will consider unusually well-qualified candidates at higher ranks. Resumes and the names of three references should be sent to Dr. R.E. Benner, Associate Chair, Department of Electrical Engineering, 3280 Merrill Engineering Bldg., University of Utah, Salt Lake City, UT 84112. Please give visa status, Screening of applicants will begin on February 15, 1992, but applications will be accepted until the position is filled. The University of Utah is an Affirmative Action/Equal Opportunity Employer and encourages nominations and applications from women and minorities.

Data Communications Engineer. Seeking qualified applicants for a full-time Data Communications Network Engineer II at private university in NE Ohio. Responsibilities are management of all communications networks including voice, video, data, telemetry and control communications; design & implementation of new services and features of communications networks, maintenance & upgrade of existing services; management of network protocols (TCP/IP, DECNET, Appletalk, SNMP, XNS [Novell]) & use of network diagnostic tools including network analyzers and time-domain reflectometers; evaluation of network performance & diagnosis of network faults; utilization of networking software (programming skills in C & Pascale languages, use & design of graphical user interfaces); use & maintenance of operating systems (Unix, MacOS, MS-DOS), Novell & Appleshare networks; design, installations & management of fiber-optic, RS232, & coaxial cabling systems; design, installation & management of data communications equipment (bridges, routers, terminal servers & computer network interfaces), design, installation & management of telephone and cable television (CATV), telemetry and control transmission equipment; technically support internal & external network communications services. Interact with other employees and vendors concerning network communications software and hardware utilizing verbal and written communications. B.S. in Electrical Engineering, Computer Science or Computer Engineering required with 2 years experience in designing, implementing & maintaining networks and/or data communications system. In lieu of B.S. and two (2) years experience; M.S. in Electrical Engineering, Computer Science or Computer Engineering, no experience required. Must have proof of legal authority to work permanently in U.S. Salary $36,847 per year; normal working hours of 37.5 hrs per week (8:30 a.m. to 5:00 p.m., Mon-

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day through Friday). Send resume, course transcript, a sample of C or Pascale program written by the candidate, and an essay on the integration of voice, video, and data communications in a campus environment in duplicate (no calls) to: J. Davies, J.O. #1255754. Ohio Bureau of Employment Services, P.O. Box 1618, Columbus, OH 43216. EEO/AA.

Chair, Electrical Engineering Department. The College of Engineering, Tennessee Technological University, is seeking a person to fill the position of Chair of the Electrical Engineering Department. Applicants should have an earned doctorate in E.E. or closely related field, be qualified for the rank of professor, have a balanced commitment to instruction and research, have excellent interpersonal and communications skills and be an effective leader in providing guidance and promoting growth in the department. Desired qualifications include administrative experience, ■ PE license or ability to acquire same, active participation in professional organizations, a record of attracting funded projects and active interaction with industries and governmental agencies. Initial screening of applicants will begin November 1, and the applicant pool will remain open until the position is filled. For information and application forms, contact R.B. Bustamante, EE Search Committee, Box 5015 TTU, Cookeville, TN 38505. Tennessee Tech is an affirmative action/equal opportunity employer. Minorities and women are encouraged to apply.

The Air Force Flight Dynamics Laboratory and The Air Force Institute of Technology announce the 1992—1994 Flight Control Distinguished Visiting Professor Program. The Air Force Institute of Technology (AFIT) at Wright-Patterson Air Force Base, Dayton, Ohio announces the opportunity to join the AFIT graduate faculty as a Distinguished Visiting Professor in the Department of Electrical and Computer Engineering in the School of Engineering. Responsibilities—The responsibilities of the AFIT Distinguished Visiting Professor include providing academic leadership in teaching and research in association with AFIT faculty and students, and initiating and conducting research and consultation with Flight Dynamics Laboratory, Air Force Wright Research and Development Center. Qualifications—The person appointed as Distinguished Visiting Professor should be an eminent faculty member at ■ prestigious university. Selection will be based upon the individual's experience, proposed teaching program and research areas. Areas of special interest and activity at AFIT are: Flight Control Systems, Control Systems for Reconfigurable Aircraft, Design of Robust Multivariable Control Systems, Quantitative Feedback Theory Design, Output Digital Feedback Design Technique for Multivariable Tracking Systems, H Control Theory, and Adaptive Control and Estimation. Applicants are expected to have a Ph.D. and be ■ professional contributor in the area of flight control. Consideration will be given to applicants who have extensive flight control experience within industry and government. Research Support—Two powerful hybrid computers (EAI Simstars) are the heart of AFIT's flight control laboratory. H high fidelity, full flight envelope, real-time aircraft simulator is developed for academic and research use. Overall, AFIT's computer resources equal or exceed those found at other universities. An office, laboratory, the use of modern computers, and other service support will be provided for the visiting professor and may include support for a limited number of the visiting professor's doctoral students. Period of Appointment and Salary—The initial period of appointment is for one full year. A shorter period and the starting date are negotiable, but should be prior to October 1, 1992. Extension for a second year may be possible. Salary is commensurate with qualifications. A per diem allowance is also paid. Application—A resume of qualifications and experience, including ■ list of significant publications and any need for support of Ph.D. students can be submitted anytime prior to December 31, 1991 to: Dr. Charles J. Bridgman, Associate Dean for Research, School of Engineering (AFIT/ENR), Air Force Institute of Technology, Wright-Patterson AFB, OH 45433-6583, Phone: (513) 255-3633. The Flight Control Distinguished Visiting Professor Program is made possible through a grant from the Air Force Wright Research and Development Center's Flight Dynamics Laboratory. AFIT is an Equal Opportunity and Affirmative Action Employer.

Research Engineers & Scientists

Digital Signal Processing

The Environmental Research Institute of Michigan (ERIM), ■ growing, leading-edge, research ■ development organization with headquarters in **Ann Arbor, MI,** has newly created opportunities for a select group of talented Research Engineers and Scientists for the following areas:

Systems:
- digital signal processing
- documentation specialist
- Kalman filtering
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- Motion compensation/ navigation systems

Software:
- Real time embedded systems
- Software testability
- Software systems engineering/ simulation/modeling
- UNIX
- User interfaces
- Algorithm Development

Hardware:
- RF and microwave design, high speed digital circuit design, microprocessor and interface technology, digital signal processor design.

Previous experience with U.S. Government programs desirable, as is ■ BS, MS or PhD in Computer Science, Electrical Engineering or Mathematics.

You'll receive ■ excellent salary with outstanding benefits and growth potential. For prompt consideration, please forward your resume in strict confidence to either: **ERIM, Box 134001, Ann Arbor, MI 48113-4001; or ERIM, 5757 West Century Blvd., Suite 340, Los Angeles, CA 90045 - Attn: Human Resources Manager-10/IEE.** ERIM has recently implemented a Doctoral Fellowship Program to promote continued technology growth and development. The program, sponsored in conjunction with the University of Michigan's Department of Electrical Engineering and Computer Science (EECS), is now accepting inquiries at the above locations.

ERIM

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Harvey Mudd College, Electrical Engineering. Applications are invited for a tenure track position (or possibly two positions) in the engineering department, beginning January or September 1992. Appointment at the Assistant or Associate Professor level is anticipated. The position(s) requires demonstrated capabilities in two or more of the following areas: analog/digital electronics, design and applications of microprocessor-based systems, signal processing and systems, VLSI, and materials. Responsibilities will include teaching in ■ unified engineering curriculum, developing courses, and supervising industrially sponsored projects in the Engineering Clinic. A doctorate is required for the position. Continuing professional growth and development through research or consulting is expected; excellent opportunities exist in the local area. Industrial experience is desirable. Reply to: Electrical Engineering Search, Attention: John I. Molinder, Chairman of Engineering, Harvey Mudd College, Claremont, CA 91711. To insure full consideration applications should be received by November 15, 1991. Harvey Mudd College is an equal opportunity/affirmative action employer.

Department of Electrical Engineering, University of Toronto. The Department of Electrical Engineering invites applications for three tenure-stream Assistant Professor positions in the following areas: 1. Communications, specializing in telecommunications and communication networks. Applicants will be knowledgeable about modern trends in telecommunications and skilled in the use of techniques related to modelling, performance analysis and simulation. 2. Electromagnetics, with intended specialization in electromagnetic compatibility and antennas. Applicants will be skilled in modern computational and experimental techniques. 3. Systems Control. Applicants should have a strong interest in the role of computers and computing in control. Experience in experimental research would be an asset. These positions involves both research and teaching at the undergraduate and graduate levels. Applicants should have a doctoral degree in Electrical Engineering, an outstanding academic record and effective teaching ability. Applicants should send ■ curriculum vitae, a statement concerning teaching and research interests, and a list of three references to: Professor Adel S. Sedra, Chair, Department of Electrical Engineering, University of Toronto, Toronto, Ontario, M5S 1A4, Canada. In accordance with Canadian Immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada. The University encourages both women and men to apply.

The Electrical Engineering Department at Christian Brothers University invites applications for tenure-track positions, available January & August 1992. Needs are in the areas of microprocessors, electronics, and telecommunications. Candidates should have a PhD/EE. Focus is on teaching, but faculty members are expected to develop opportunities for scholarly activities. Send resumes and names of three references to: Brother Louis Althaus, Head, Electrical Engineering, CBU, Memphis, TN 38104 AA/EO Employer.

The Department of Electrical and Computer Engineering at the University of the Pacific is accepting applications for ■ tenure-track position at the Assistant or Associate Professor level. Candidates should have ■ Ph.D.; also some industrial experience is desirable. Preference will be given to individuals with expertise in the areas of computer engineering and electronics. Undergraduate education is the primary responsibility; curriculum development, advising, MS-level teaching and clinic supervision, and scholarly activity/research are also expected. UOP is ■ private, comprehensive university

Deputy Director for Spectrum

The U.S. Department of Commerce, National Telecommunications and Information Administration, Institute for Telecommunication Sciences, Boulder, Colorado, is seeking a Senior Electronics Engineer to lead its Spectrum Division, one of two technical divisions within the Institute; the other being the Systems and Networks Division.

The Spectrum Division is responsible for research and investigation leading to the acquisition, analysis, and publication of information concerning the propagation of electromagnetic waves at all frequencies along the surface of the earth, in the atmosphere and in space; the nature of electromagnetic noise and interference; and the methods for more efficient use of the electromagnetic spectrum for telecommunication purposes.

The individual should have extensive experience in radio spectrum measurement and model development, and radio system standards development and advocacy leading to support of national needs in telecommunications. Substantial physics or engineering background is required as well as demonstrated experience in managing research activities.

The position is full-time permanent; with an annual salary between $87,000 to $108,300.

For further information and application forms, please contact Nancy Thornton of the Personnel Office at (303) 497-3972 or DOC/MASC, MC 23, (Thornton), 325 Broadway, Boulder, Colorado 80303.

U. S. Citizenship is required.
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High-Temperature Superconductors is published monthly on a calendar year basis, at a 1991 subscription price of **$142** per annum (**$79** for members of IEE, IEEE, IOP, BCS, AIP). (Prepayment is required).

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Thomson Consumer Electronics, designer and manufacturer of RCA and GE brand consumer electronics products, is a global leader in the development of new television technologies. Our Indianapolis advanced development facility, an integral part of our worldwide network of R&D labs, has immediate opportunities for experienced microcomputer engineers to join our TV Control Systems development group.

Qualifications must include a BS (or advanced degree) in Electrical Engineering, and a solid background in computer science/engineering. Experience in designing with embedded microcomputers is essential. In addition to microcomputer hardware, a high proficiency in assembly and high level languages such as "C" is required.

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with a total enrollment of approximately 3800 students. Send resume to: Dr. Richard H. Turpin, Electrical and Computer Engineering, University of the Pacific, Stockton, CA 95211. UOP is an Equal Opportunity/Affirmative Action Employer.

Electrical Engineering: Trinity University. The Engineering Science Department invites applications for a tenure track assistant professorship. Qualifications include the Ph.D. or equivalent in Electrical Engineering, a genuine interest in high quality undergraduate teaching and advising, and the ability to develop and maintain research (preferably with undergraduate involvement). Teaching areas include: design; circuits, electronics and microprocessor applications; control systems and robotics; and instrumentation/manufacturing. P.E. or willingness to obtain same is very desirable. Nine full-time faculty teach in this accredited, interdisciplinary program which offers some specialization in chemical, electrical, and mechanical engineering. Women and minorities are urged to apply: TU is an EO/AA employer. Submit resume, visa status and three references by 1 Jan 92 to: Dr. H. William Collins, Dept. of Engineering Science, Trinity University, 715 Stadium Drive, San Antonio, TX 78212, (512) 736-7511.

The Electrical Engineering Technology Department of Purdue University announces anticipated academic-year tenure-track position at West Lafayette, Anderson, Columbus, Kokomo, New Albany, and South Bend, Indiana, commencing January 2, 1992, or August 17, 1992. Minimum requirements are: a master's degree in electrical engineering, electrical engineering technology, or a closely related field; three years of recent relevant industrial experience; a strong commitment to undergraduate teaching. Applicants must have expertise in at least two specialty areas. Candidates from industry, engineering technology programs, or strong community college technical programs are encouraged to apply. In addition to teaching, faculty are expected to engage in curriculum development, some program coordination, student advising, take an active role on departmental or university committees, and to pursue scholarly activity by publishing and participating in professional society meetings. For priority consideration, applications should be submitted by November 22, 1991, for January, 1992 appointment, or by February 14, 1992, for August, 1992 appointments. The positions will remain open until they are filled. Send a detailed resume, the names, addresses and phone numbers of three references, and your location preferences to: Prof. W. Frank Reeve, Chairman, Faculty Search Committee, Electrical Engineering Technology Department, Knoy Hall, Purdue University, West Lafayette, IN 47907. Purdue is an equal opportunity/affirmative action employer.

Clarkson University, Electrical and Computer Engineering. Applications are invited for a tenure-track faculty position as Assistant/Associate/Full Professor in electrical engineering or computer engineering. Responsibilities include undergraduate and graduate teaching and development of a research program. A doctorate is required. Review of applications will begin on November 30th and will continue until the position is filled. The department, consisting of 28 faculty members, offers programs at the B.S., M.S., and Ph.D. levels. Last year 122 EE bachelors, 20 CE bachelors, 15 masters, and 9 doctorate were awarded, and research funding reached more than one million dollars. Principle research areas include distributed and parallel computation, artificial intelligence, image and signal processing, neural networks, robotics and control, communication systems, solid state devices, electromagnetic scattering, power systems, and electromagnetic devices. There are research labs in artificial intelligence and neural computing, VLSI design, robotics, lasers and optics, solid state device fabrication, high voltage engineering, and dielectric breakdown. Clarkson is an independent university specializing in engineering, science and management with an enrollment of 3300 students, including 400 graduate students. Located in northern New York, Clarkson is close to Lake Placid and the Adirondack Mountains. Send applications to Professor Henry Domingos, Chairman, Department of Electrical and Computer Engineering, Clarkson University, Potsdam, New York 13699-5720. Clarkson is an Equal Opportunity/Affirmative Action Employer. Position No. 245.

University of Texas at Arlington. The Department of Electrical Engineering invites applications for tenure-track faculty positions in the following areas: digital systems with special emphasis on signal processors, parallel processors and microprocessor interfaces; remote sensing and wave scattering; and high speed electronics with emphasis in the design, fabrication, and characterization of microwave, millimeter-wave, and optoelectronic devices and circuits based on compound semiconductors. A Ph.D. and a background in electrical engineering is required. The department presently has 30 faculty and produces 150 BS, 110 MS and 12 PhDs annually. It has an annual research volume of $3M. The university is located in the heart of the Dallas/Ft. Worth metroplex, 30 miles north of the site of the superconducting super collider. Please send resume to Professor Robert Mitchell, Department of Electrical Engineering, University of Texas at Arlington, Box 19016, Arlington, Texas 76019-0016. The University of Texas at Arlington is an Equal Opportunity/Affirmative Action Employer.

Faculty Position in Devices-Caltech. The Electrical Engineering program at Caltech invites applications for a tenure-track position as assistant professor. The term of the initial appointment is normally four years, and is contingent on completion of Ph.D. requirements. Exceptionally well qualified applicants may also be considered at the assistant for full professor level. Candidates with interests in electronic, magnetics, acoustic, optical, or superconducting devices, and sensors, are encouraged to apply. We are seeking a highly qualified candidate who is committed to a career in research and teaching. Interested applicants should submit a resume with the names and mailing addresses of at least three references to Professor David Rutledge, Department of Electrical Engineering, California institute of Technology, Pasadena, CA 91125. Caltech is an Equal Opportunity/Affirmative Action Employer. Women and minorities are encouraged to apply.

Department of Industrial & Operations Engineering University of Michigan. The Department of Industrial and Operations Engineering at the University of Michigan anticipates one to two tenured or tenure-track faculty openings for September 1992. Appointments at all ranks will be considered. Candidates should have research and teaching interests in at least one of the following areas: 1. Engineering and technology management -strategic management of technology, economic analysis, capital planning, R&D management, and related areas. 2. Quantitative modeling of decision making and problem solving under risk and uncertainty—risk taking behavior in manufacturing and service operations, individual risk taking behavior, group problem solving, computer-based decision support, and related areas. 3. Manufacturing and distribution systems—quality assurance, production planning and control, concurrent engineering, throughput and process control, and related areas. 4. Statistics - quality control, reliability of manufacturing and service systems, simulation, and related areas. Applicants with interdisciplinary interests are especially encouraged to apply. Of particular interest are candidates with research and/or teaching capabilities in the information systems aspects of the above areas. Applicants should possess or be near completion of a Ph.D. in Industrial Engineering or a related field. An established record of publications, leadership, and sponsored research is required for appointment at the senior ranks. Operational experience or an engineering and/or implementation orientation is required at all ranks. The University of Michigan is an equal opportunity, affirmative action employer. Send inquiries and current resume to: Chair, Faculty Search Committee, Department of Industrial & Operations Engineering, University of Michigan, Ann Arbor, Michigan 48109-2117.

University of Washington. The Department of Electrical Engineering of the University of Washington invites applications for a

nontenure-track research faculty position in the area of imaging and graphics systems oriented towards highly-integrated multimedia systems with high processing rates. A doctorate in electrical or computer engineering, with research experience in image computing and systems, is required. Applicants must have experience in the following areas: image processing and graphics hardware and algorithms, high-performance (parallel and pipelined) computer systems, high-speed circuit design and simulation, and VLSI design. A knowledge of the theoretical and practical considerations involved in the design and fabrication of special-purpose VLSI integrated circuits and systems, as well as actual experience with the implementation of VLSI and imaging hardware and software, is also desirable. Applicants should send a detailed resume and the names and addresses of at least four references to Yongmin Kim, Professor and Director of Image Computing Systems Laboratory, Department of Electrical Engineering, University of Washington, FT-10, Seattle, Washington 98195. The University of Washington is an equal opportunity/affirmative action employer.

The Mechanical Engineering Department at Carnegie Mellon University invites applications for tenure-track positions at the Assistant Professor level commencing September 1992 in the following areas: 1. Robotics and Controls (2), 2. Solid Mechanics (1). One of the controls positions is joint with the Robotics Institute at Carnegie Mellon. Applicants must have a Ph.D. in Mechanical Engineering (or closely related field). Duties include teaching undergraduate and graduate courses, and research. Appointments at a higher rank will be considered for qualified applicants having a proven record of grant support. Submit application, complete resume, and names of three references to Professor G.B. Sinclair, Mechanical Engineering Department, Carnegie Mellon University, Schenley Park, Pittsburgh, PA 15213-3890. Closing date for applications is January 31, 1992. Carnegie Mellon University is an affirmative action/equal opportunity employer.

Digital Image Processing/Program Development (91/11/30-2) 1-yr pstn, create program/digitally process images of visual impact of reduced visibility on scenic vistas, pub and present results. BS in EE, CS, or rel. field w/emph. in dig. image proc. reqd; adv deg desble. Exp w/photo concepts, VAX/VMS, DOS, C, Fortran reqd; univ/multivariate stat, RadTran thry, Solitaire film writer and Howtec digitizer desrble. Salary commens with qualfctns. Send ltr of ap & res to Prof Thomas Vonder Haar, CIRA-Foothills Campus, CSU, Ft Collins, CO 80523. CSU is an EEO/AA employer. EO office: 314 Student Serv Bldg.

Trinity College seeks applicants for a tenure-track assistant professorship in Mechnical Engineering starting in Fall, 1992. A Ph.D. in M.E. with primary expertise in thermodynamcis and heat transfer is required. Trinity offers a standard M.E. curriculum within a liberal arts setting. The new Mathematics, Computing, and Engineering Center houses laboratories for instruction and research in solid mechanics, materials science, fluid mechanics, electronics, and electrophysiology. Networked computers include micros, workstations, and mainframes. Send a curriculum vita, a statement of teaching and research objectives, copies of publications (optional), and the names of three references to Dr. David J. Ahlgren, Chair, Engineering and Computer Science, Trinity College, Hartford, CT 06106. We especially seek applications from women and minority candidates. Applications accepted until January 10, 1992. Trinity College is an AA/EO employer.

Government/Industry Positions Open

Research Engineer. Research, development and implementation of new speech compression algorithms using digital signal processing techniques and DSP processors. Requires PhD in Electrical Engineering and completion of graduate courses in Random Processes, Detection and Estimation, Analog and Digital Communications. Must be conversant with expontential data fitting as evidence by PhD dissertation. Requires 2 years experience in job offered or in research in Spectrum Estimation. $1,050/wk, 40 hrs/wk. Place of employment and interview: Cupertino, CA. Send this ad and resume to Job #PM 10370, P.O. Box 9560, Sacramento, CA 95823-0560 no later than 10-31-91.

Electronics Research Engineer—To develop and implement hardware and software accurate performance mathematical models to characterize the overall system availability and reliability; to develop processes to improve the quality of fault tolerant packet switching systems used in domestic and international intelligent networks. Requires a PhD in Electrical and/or Computer Engineering. Applicant must also have 2 years experience in job offered or as a research associate in modeling and simulation of complex hardware and software systems in the Electrical and Computer Engineering Department at a college/university with experience in computer simulation, hardware and software systems, control systems mathematics and statistics. Graduate level courses in hardware and control systems and probability and statistics are required. Dissertation topic related to "switching systems" is also required. Experience may be gained before, during or after degree. 40 hours per week, (work schedule, 8:00 am to 5:00 pm). Salary is $59,000 per year. Must have proof of legal authority to work permanently in the U.S. Send resume in duplicate (No calls) to: S. Holton, JO #1260304, Ohio Bureau of Employment Services, P.O. Box 1618, Columbus, OH 43216.

Corporate Project Engineer Sought at Kraft Mill, Tacoma, Washington. Applicant must be abe to: (1) Provide engineering expertise in the design and implementation of a computerized distributive control system for the safe and efficient generation of electrical power at the Kraft Mill. (2) Increase the reliability and technical performance of the utilities plant to a level that is consistent with accepted operating criteria and good housekeeping practices. (3) For the maintenance and operating departments, help prepare, recommend, implement and review long-range plans, budgets and operating strategies to agreed upon costs and operating efficiency objectives. (4) Assist the corporate project engineer assigned to the Kraft Mill to manage and coordinate capital projects to assure timely and cost-effective completion. (5) Manage and coordinate all aspects of implementing the approval projects, including engineering equipment selection, construction, cost control, start-up and training. (6) Supervise contractors of multiple crafts on major maintenance projects during the semiannual mill-wide shutdown time. (7) Assume responsibility for effective utilization of capital funds by evaluating project proposals and translating them into economically and technically feasible projects. (8) Assist in the preparation of the annual budget. Applicant must have proficient verbal and written communication skills. Extensive overtime is required on holidays and during project start-ups. Must have Masters Degree in Engineering or equivalent experience and five years of experience in the pulp and paper industry or five years of indirect experience where knowledge gained can be applied to the pulp and paper industry. 40 hours/week. Salary $4,800/month. Must have legal authority to work permanently in the United States. Send resume by October 31, 1991 to Employment Security Department, Employment Service Division, Attn: AEC Unit, Job No. WA 0274911J, Olympia, Washington 98504.

Senior Research Scientist—Perform independent research, conceptualization, proposal writing, analysis and design of data management in distributed systems, real-time/control systems. Using object-oriented languages and databases. Position requires real-time database software design, implementation and performance evaluation. Assist in new project development and development and testing of product prototypes in the areas of electric control systems and software engineering tools. Requires PhD degree in Computer Science/Engineering. Candidate must have sound research background evidenced by publications in the areas of database systems, real-time systems and real-time database systems. Evidence of design, construction and implementation of actual real-time database systems. Must have demonstrated the ability to write proposals and give technical presentations. Requires at least one year industrial experience in industrial control and the design and implementation of microprocessor-based control systems and interfaces. Requires at least one year experience in the use of one or more DBMS's, including schema design and user-interface implementation. Educational background must include extensive experience, as evidenced by system implementation, with operating systems, including VMS, and strong programming skills, including C and assembly languages. Must be familiar with distributed systems and credit graduate level exposure or one year equivalent industry experience in the areas of computer architecture, computer aided design, performance evaluation, real-time systems, computer network and distributed processing as well as database design and implementation. Salary $56,000 per year. Submit resumes to: Ms. S. Springmeyer, MDJT/ALCU # 1-191, 390 North Robert Street, Room 124, St. Paul, MN 55101.

Object Database Staff Engineer. Research and development of relational and object oriented Database Management System using knowledge of commercial and research object oriented database systems in order to provide production direction. Consult with managers and other engineers in the area of formal definition of object oriented database interfaces. Work on the Distributed Computer Model Project using knowledge of parallel computer architecture and parallel processing. Ph.D. in Electrical Engineering with major in Object Oriented Database plus four years research experience in parallel computer architecture and parallel processing required. 40 hour work week—8:00 a.m. to 5:00 p.m.—$56,400/year. Qualified applicants send resume or application letter with ad within twenty (20) days from date of initial publication to: AZ DES, Job Service, Attn: 732-A, Re: 0752144, P.O. Box 6123, Phoenix, AZ 85005-6123. (Job location: Phoenix) Employer paid ad. Proof of authorization to accept permanent full-time employment in the U.S. required if hired.

Process Engineer, Senior. Define, execute, characterize & evaluate process development experiments to develop & enhance manufacturable sub-micron CMOS & BiCMOS processes; conduct process & device simulation and electrical measurement of test structures & technology specific devices; extract device parameters & develop models to explain data; oversee & direct materials, defect & physical characterization of processes for yield modeling & analysis. Ph.D. in Electrical Engineering, Physics or Materials Science. Academic project/research background in silicon semiconductor process/device development, including process definition & characterization, process modeling, device characterization, process & device simulation using SUPREM & PISCES, surface analytical techniques including SIMS or SEM, and sample preparation; academic coursework in electronic materials, IC fabrication and semiconductor devices. $4,600/mo.; 40 hrs./wk. Place of employment and interview: Santa Clara, CA. If offered employment, must show legal right to work. Clip ad and send with resume to: Job No. MD #21333, P.O. Box 9560, Sacramento, CA 95823-0560 not later than October 31, 1991. The company is an equal opportunity employer and fully supports affirmative action practices.

Staff Project Engineer/Electrical Design Engineer; 40 hours/week. 8:00 am-4:30 pm; $5,417/month. Overtime as needed, not compensated. Job requires: Bachelor's degree in Electrical Engineering and 6 years experience as an Electrical Engineer. Job also requires: 1) Experience must include 6 years experience designing software systems for real-time multi-microcomputer control systems; 2) Experience must include 6 years experience configuring hardware modules and designing interfaces in a new technology manufacturing environment; 3) Experience must include 6 years experience reviewing and evaluating technical designs of vendors or other design groups; 4) Experience must include 2 years experience optimizing mechanical designs for manufacturing and assembly as well as mass and cost reductions; and 5) Experience must include 2 years experience coding and debugging software written in a microcomputer assembly language. Special requirements 1), 2), 3), 4), and 5) may be met concurrently during the same 6-year periods. Job duties: work as a senior design and

reliability engineer for Electric Vehicle Program. Design and develop the architecture of the vehicle microcomputer control modules and the functional partitioning of the required control systems. Technically review the designs of several components vendors involved in developing the vehicle computer control modules. Ensure that the microcomputer module interface design is coherent, reliable, and fail safe. Review and supervise the maintenance of all electrical technical specification documentation at the vehicle, subsystem, and component levels. Analyze and predict the reliability of the vehicle electrical subsystems and components. Develop and review design modifications to ensure optimal reliability without compromising manufacturability, assembly, mass, and cost. Plan, design, and develop the electrical systems architecture and reliability for future electrical vehicles. Qualified applicants should send resume and verification of requirements to: 7310 Woodward, Room 415, Detroit, MI 48202. Reference #57491. Employer Paid Ad. An Equal Opportunity Employment-paid Advertisement.

Network Software Systems Engineer needed by company in Denver, CO which manufactures and sells computers. Provide in-house systems engineering for communications network control being developed for VAX 8600. Support Network Manager by evaluating change proposals, reviewing software designs, and examining test results. Participate in hardware/software system tests and RF interference analysis. Requires BS in Engineering; 2 years experience as engineer working with VAX/VMS workstations and 386 PCs network architecture design; working knowledge of multi-vendor network architecture planning, installation and debugging; working knowledge of high-speed network interface circuitry design and RF interference tests to assure compliance with FCC regulations $35,000/year; 8:30am-5:30pm, M-F. Respond by resume no later than October 30, 1991 to Colorado Department of Labor & Employment, Division of Employment & Training, 600 Grant, Suite 900, Denver, CO 80203, ATT: James Shimada, and refer to Job Order No. CO3773838.

Research Staff Member: Performs original research on high performance I/O systems with the focus on storage subsystems such as disk arrays. Conceives new algorithms & machine organizations that will improve the subsystems characteristics such as: performance, fault-tolerant, & cost. Develops, simulates & analyzes models of such subsystems. Architects, designs, implements, instruments & tests prototypes to verify the accuracy of select models in real situations. Writes conference papers, journal articles & internal reports about the results. Provides consultation to others in area of expertise. Requires: PhD in Computer Engineering with emphasis on high performance I/O architecture; famil. w/disk array design issues; famil. w/fault-tolerant computing design issues; abil. to do performance analysis; & famil. w/multiprocessor & parallel processing design issues. The above may be demonstrated through PhD dissertation. 40 hrs./week; $62,500/year. Job & interview site: San Jose, CA. Send this ad & your resume to Job #PC 20306, P.O. Box 9560, Sacramento, CA 95823-0560 not later than October 30, 1991. EOE.

Research Staff member: Will conduct research rel. to micromachines, focusing on appl. of these device to info. storage. Will conduct research in surface machining tech. & characterization of mechanical & electromagnetic properties of thin films, tailoring these properties thru modif. of thin-film processors. Must initially identify key research issues & estab. lab. to conduct indep., adv. research in this area, requiring formulation of research plans, acquisition & set-up of neces. lab. equipment, & estab. of collaborative working relationships w/colleagues in other research groups. Will represent co. in int'l conferences rel. to above. Research activ. directed towards develop. of patentable inventions which extend the technology. Req'd. to publish results to orig. research in scholarly journals & internal tech. pubs. Reqs. Ph.D. in C.S., EE, or rel., &: (1) Ph.D. level experimentation in ■ all of following areas rel. to micromachining of microdynamic structures: in situ. assembly technology, thin-film material properties, & integrated microactuators; (2) recent publ. in scholarly journals of articles in areas rel. to foregoing; (3) high level of expertise in micromechanics/micrfabrications, to be demons. thru talks, selection as session chairperson, proceeding editor, or equiv.; (4) completion of advanced research in silicon surface micromachining & thin film processing/characterization & in TEM & X-ray analysis; (5) authorship on inter-discipl. papers; (6) knowl. of safety requirements for working w/silane, phosphene, & other hazardous materials. 40 hrs./wk., $4910/mo. Job & interview site: San Jose, CA. Send this ad & your resume to Job ■ EG 14203, P.O. Box 9560, Sacramento, CA 95823-0560 not later than October 30, 1991. EOE.

Project Engineer; 40 hours/week; 8:00 a.m.—4:30 p.m.; $43,500/year. Job requires: Master's degree in Electrical Engineering and 3 years experience as an Electrical Engineer and/or as a University Research Assistant. Job also requires: 1) Experience must include 6 months experience developing and implementing digital signal processor-based real-time systems; 2) Experience must include 6 months experience using Motorola and Texas Instruments DSP assembly languages and C language; 3) Research which includes application of adaptive signal processing methods to an acoustic system utilizing digital signal processor(s) as evidenced by Master's thesis; and 4) 1 grad. course in each of the following: a) adaptive signal processing; b) parallel processing; c) microprocessor system design; and d) digital signal processors. Special requirements 1) and 2) may be met concurrently during the same time period. Job duties: Design and implement digital signal processor-based control systems for automotive applications with emphasis on noise and vibrations applications. Perform system analysis and simulation. Develop and implement algorithms. Test and evaluate prototype system in laboratory and vehicle environments. Qualified applicants should send resume and verification of requirements to: 7310 Woodward, Room 415, Detroit, MI 48202. Reference #63091. Employer Paid Ad. An Equal Opportunity Employment-Paid Advertisement.

Careers in Patent Law—Morgan & Finnegan, ■ 100-year old intellectual property law firm with offices in mid-town Manhattan and Washington, D.C. seeks electrical engineers with at leas tan EE degree and an interest in patent and technology-related law. Full-time employment includes training to become a registered U.S. Patent Agent, preparing and prosecuting patent application and serving as scientific advisors in litigations and in counseling our sophisticated electronics clients. We offer an excellent salary and benefits package. Send resumes in confidence to Kathy Louros, Recruiting Coordinator, Morgan & Finnegan, 345 Park Avenue, New York, NY 10154.

Electronic Engineer—A Michigan affiliate of ■ European based company is engaged in the manufacturing and importing of metal forming presses and press lines. the company has an immediate need for an Electronic Engineer to take responsibility for designing electronic control systems. adapting the original control systems to American standards and to customer requirements, supervising and coordinating production of Muller-Weingarten die casting machines, hydraulic presses and small screw presses, writing and upgrading programs for Siemens PLC controls, engineering services support for Allan Bradley PLC controls, engineering service support for customers for Muller-Weingarten hydraulic presses, blanking lines, automated feeder systems, die casting equipment, notching presses; training U.S. customers in electronic/electrical controls, hydraulics and mechanics of Muller-Weingarten products. Minimum requirement include at least a bachelor's of science degree in engineering with a major in electronics, six years experience as an electronic engineering and one year experience as an electrical engineer. three of the six years experience must by with Muller-Weingarten 2000, 1200 and 800 ton hydraulic presses, blanking lines, feeder systems and Siemens motor drives and Siemens PLC controls. Must have experience with programmable controllers. Starting salary is $45,000 per year. the work schedule is 9:00 am to 5:00 pm for a forty hour week. Qualified applicants respond with two (2) copies of resume to: 7310 Woodward Ave., Room 415, Detroit, MI 48202, Ref., No. 17991. Employer Paid Ad.

Senior Device Engineer. Resp. for yield enhancement eng. & analytical characterization on ASIC & Logic products. Resp. incls. micron & submicron process & device analysis, process control monitor design, physical defect analysis , & advanced technology introduction & stabilization, using such tools as adhoc yield modeling, surface & sub-surface particulate & residual composition analysis (SEM, Auger & secondary electron, X-ray photoelectron & secondary ion mass spectroscopy). Reqs. M.S. in EE & 3 yrs of exp. in ASIC device eng. or a PhD in EE or Solid State Physics (concentrating in submicron process development, device design, fabrication, & characterization) may substitute for industrial experience. Also reqs. exp. or research background & knowl. of: semiconductor device physics incl. exp. modeling influence of process techniques & equipment on devices & circuit performance in submicron VLSI processes & Transport physics in submicron devices; semiconductor processing, & equipment; process & device modeling & simulation; device & circuit test, measurement tools & techniques. Also reqs. knowl. of computer systems & software used for CAD & modeling incl. knowl. of VAX?VMS & Unix workstations; knowl. of experimental design & process/device parameter control using statistical analysis; & understanding of semiconductor chemistry & surface/interface analysis & background using scanning/ transmission electron microscope, energy dispersive x-ray analysis & ion mass spectroscopy. Salary: $52,410/yr. Job site: San Antonio, TX. Apply at the Texas Employment Commission, Dallas, Texas, or send resume to the Texas Employment Commission, TEC Building, Austin, Texas 78778, J.O. # 6421962. Ad paid by An Equal Employment Opportunity Employer.

Field Engineer for elect. controls mftr in Cleveland, OH, to design & coordinate integration of machinery & microprocessor-based control equipment into mftr process periodically modifying to conform to technological upgrades in machinery & equipment. Provide tech support including modeling & applications of software & support of hardware. Responsible for installation & commissioning of microprocessor-based converter drive equipment. Train other employees in troubleshooting & maintenance procedures of equipment. Requires BS or equivalent in Electrical Engineering, Computer Science or Computer Systems & either 2 yrs. exp in job described or 2 yrs exp in applications, systems or commissioning engineering or in elect. tech apprenticeship. Exp must include working with GEM 80 microprocessor-based programmable controller in both systems design & applications 40hrs/wk, 8am-5pm, Mon-Fri, $51,000 per yr. Must have proof of legal authority to work permanently in U.S. Send resume in duplicate (no calls) to J. Davies, JO#1255789, Ohio Bureau of Employment Services, PO Box 1618, Columbus, OH 43216.

Electronics Engineer—Voice Quality Research. The U.S. Department of Commerce, National Telecommunications and Information Administration, Institute for Telecommunication Sciences, Boulder, Colorado, is seeking an Electronics Engineer to lead a program in voice Quality Research. This position requires: (1) A degree in engineering or equivalent; (2) Knowledge of statistical cojmmunication theory, statistical pattern recognition, signal and image processing, information theory, data communication, probability, random processes and statistics; (3) Knowledge of subjective and objective quality testing of voice signals; (4) Experience with national and international standards organizations; (5) Telephony background; (6) Proficiency in computer programming using C, Fortran and Pascal on MS-DOS and Unix based mini and micro computers; (7) Project leadership experience. The position is full-time permanent and is located in Boulder, Colorado. Annual salary may be $52,406–$68,129 (GS-14). For further information and application forms, please contact Kathy Dolan, of the Personnel Office at (303) 497-3973 or DOC/MASC, MC 25, (Dolan), 325 Broadway, Boulder, Colorado 80303. Refer to Vacancy Announcement MASC/NITA 91-307. U.S. Citizenship is required. Equal Opportunity Employer.

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POSIX encompasses a range of standards under development by the IEEE to provide interfaces for application portability across multiple hardware and software platforms. Virtually every computer supplier and open systems specifier has adopted POSIX.

Future IEEE standards considered within the POSIX family include: Shell and Utility Facilities; C, Ada, and FORTRAN Bindings; Networking Protocols; Real-time Extensions; and Verification Testing.

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The engineer at large

PEs may rejoin engineering societies

The National Society of Professional Engineers (NSPE) may rejoin the American Association of Engineering Societies (AAES), which the 75 000-member-strong NSPE quit in 1989. The rejoining is conditional, however, on a restructuring of the AAES that NSPE believes would strengthen its image as representative of the entire engineering community, particularly in efforts to influence the public policy arena in Washington, D.C. AAES would grant individual membership to all members of the engineering societies belonging to it, currently more than 500 000 members of the 22 societies.

Other proposed changes, which the presidents of the AAES engineering societies have agreed to consider, involve how the AAES is governed. A letter sent to the AAES on behalf of IEEE President Eric Sumner and AAES Governor Merrill Buckley Jr. (IEEE President-Elect) states that the IEEE "agrees in principle to the proposal to restructure the AAES to achieve engineering unity."

Call for Baldrige Award examiners

The National Institute of Standards and Technology (NIST) is looking for examiners who will review and evaluate applications for the 1992 Malcolm Baldrige National Quality Award. Established by the U.S. Congress in 1987, the award seeks to promote quality awareness of products and services of U.S. companies, to recognize the firms' quality achievements, and to publicize successful quality strategies. The award is conferred on a company for its effectiveness in this area, not for its products and services alone.

Would-be examiners must be expert in quality management and able to evaluate large and small manufacturing and service businesses. *Contact: Malcolm Baldrige National Quality Award Office, A537 Administration Building, National Institute of Standards and Technology, Gaithersburg, Md. 20899; 301-975-2036.*

Better pay for graduating engineers

Whether the U.S. economy is recovering or not remains open to question, but this year's engineering school graduates were offered higher starting salaries than their peers were offered last year. Electrical engineers placed fourth with an average annual salary offer of US $33 191, according to a salary survey conducted by the College Placement Council, based in Bethlehem, Pa., and reported in July. This average represented a 4.4 percent boost over the average of starting offers made to new graduates through September 1990.

Engineers in the petroleum and chemical industries were courted most heavily. Over last year, the average salary offered to petroleum engineers jumped 10.7 percent to $38 972, while the offer to chemical engineers increased 6.4 percent to $37 381. Just ahead of the EEs were those in mechanical engineering, whose average starting salary rose 6.1 percent to $34 007.

COORDINATOR: Alfred Rosenblatt

Legal aspects

Japan and United States renew semiconductor pact

Joel Miller

Front-page news was made earlier this year by an agreement between Japan and the United States over memory chips and other electronic components. The renewal of a five-year-old accord, it has generated much interest and some controversy among chip makers, computer manufacturers, and economists. A significant difference from its predecessor is the new agreement's mechanism for monitoring semiconductor prices.

THE QUEST FOR MARKET SHARE. Back in the mid-1980s, U.S. semiconductor firms believed that Japanese manufacturers were selling chips in the United States at unfairly low prices. They also believed they faced insurmountable obstacles to selling their products in the Japanese market.

To remedy matters, three proceedings were brought under U.S. trade laws: an action to improve access to the Japanese semiconductor market, and two investigations into memory chip pricing and possible "dumping." According to the United States Code, Title 19, Section 1673, dumping is the sale of a foreign-made product in the United States at less than fair value (that is, less than the price charged in the home market, in this instance, Japan) where such sales threaten to harm U.S. industry.

The first proceeding was brought at the request of the Semiconductor Industry Association (SIA), of Cupertino, Calif. The trade group claimed that U.S. firms were being denied opportunities to sell their products in Japan on an equal footing with Japanese firms, and wanted the U.S. government to intercede under the authority of Section 301 of the trade statutes (Section 2411 in the United States Code, Title 19). This provision authorizes the Federal government to investigate and seek the elimination of other nations' acts, policies, and practices judged discriminatory or inconsistent with existing trade agreements.

The two dumping proceedings were conducted jointly by the U.S. International Trade Commission and the Department of Commerce. One was brought at the SIA's request and focused upon sales of erasable programmable ROMs (EPROMs). The other, concerned with dynamic RAMs (DRAMs) having 256K-bit densities and up, was initiated by the Commerce Department.

SPEEDY RESOLUTION. The investigations moved quickly. Rather than being solved individually, all three were disposed of in one 1986 agreement, the "Arrangement between the Government of Japan and the Government of the United States concerning Trade in Semiconductor Products," which achieved two major objectives. First, Japan agreed to improve U.S. access to the Japanese semiconductor market. Second, the United States agreed to suspend the two dumping proceedings in return for Japan's promise to maintain U.S. prices of DRAMs and EPROMs at or above foreign market values, and to monitor prices of those components on a worldwide basis.

This last provision drew criticism from the European Community, which objected to the agreement as a violation of the General Agreement on Tariffs and Trade (GATT). It took the position that monitoring of Japanese parts sold in countries other than the United States interfered unduly with the markets of those nations. It claimed, too, that an agreement to improve the market share of U.S. suppliers in Japan discriminated against non-U.S. firms also fighting for a foothold there.

A GATT panel subsequently found merit in the first argument, but not the second, whereupon Japan agreed to modify its monitoring procedures.

ARRANGEMENT II. The 1986 arrangement expired on July 31, 1991. Toward the end of its term, the pros and cons of continuing it were hotly debated. Ultimately, after several months of negotiation and industry comment, on June 11, 1991, Japan and the United States arrived at a successor agreement.

The five-year 1991 arrangement went into effect this past Aug. 1. Like its predecessor, it aims at enhancing access to the Japanese semiconductor market and deterring dumping. On dumping, though, the new agreement differs from the original in that it does not state minimum prices for components sold in the United States. Instead, Japanese semiconductor manufacturers will themselves monitor their output and pricing, lessening Government involvement.

The 1991 accord also provides for design-ins, the development of new semiconductor devices for use in future Japanese products. This last element may offer additional opportunities for U.S. chip designers.

It is too early to predict the full impact of the 1991 arrangement over the next five years. However, several Japanese chip makers are already warning that it will trigger a price increase—even though the new agreement avoids the minimum pricing that indirectly and unexpectedly triggered a steep price rise after the 1986 pact.

Joel Miller is an attorney in private practice in West Orange, N.J.

COORDINATOR: Trudy E. Bell

EEs' tools & toys

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The Electrical Engineering Pac sells for US $99.95. *Contact: Alan S. Fudge, Sparcom Corp., 897 N.W. Grant Ave., Corvallis, Ore. 97330; 503-757-8416; fax, 503-753-7821; or* **circle 101.**

SOFTWARE

Free demo graphics disk

Want to try your hand at using Axum, a technical graphics and data analysis package for IBM Corp. personal computers? A demo diskette for it combines two- and three-dimensional and contour plotting with data analysis capabilities within a windowing and menuing environment. Data can be analyzed and edited and then reproduced in publication-quality graphs.

The software requires an IBM-PC/XT/AT or PS/2 or compatible with hard disk, computer graphics card, and DOS 3.0 or above. The demo disk is free, but the suggested price of the software, available on a 5.25- or 3.5-inch diskette for EGA or VGA graphics, is $495. *Contact: Lee E. Edlefsen, TriMetrix Inc., 444 N.E. Ravenna Blvd., #210, Seattle, Wash. 98115; 800-548-5643; in Washington State, call 206-527-1801; fax, 206-522-9159; or* **circle 102.**

SOCIOTECHNOLOGY

Men, machines, and history

History buffs can now purchase a set of over 500 transcripts chronicling scientific and engineering events. The transcripts, taken from "Engines of Our Ingenuity," a nationally syndicated radio program broadcast daily on National Public Radio stations in over 30 U.S. cities, are available on up to six diskettes in 3.5- and 5.25-inch DOS formats, and in Hypercard format for the Macintosh, for US $20 per set. Also available for $5 each are audiocassettes containing seven programs.

The three-to-five-minute-long programs, salute "the machines that make our civilization run, and the people whose ingenuity created them." *Contact: Richard Boswell, Stress Engineering Services Inc., 13800 Westfair Dr., Houston, Texas 77041; 713-955-2900; fax, 713-955-2638.*

TOY

Astronomy software list

Over 150 astronomy computer programs are voluminously described in an annotated list organized by software type. It includes simulations, planetaria (or star charts), calculation aids, games, telescope and observing aids, tutorials, and solar system displays.

Also included are addresses and telephone numbers of vendors and sources, and an introductory reading list of books and articles about astronomical software. For a copy of the 10-page packet, send a donation of $4 to cover printing, mailing, and handling. Make that $7 if you're outside the United States. *Contact: Astronomical Society of the Pacific, Software List Department, 390 Ashton Ave., San Francisco, Calif. 94112; 415-337-1100; fax, 415-337-5205; or* **circle 103.**

COORDINATOR: Alfred Rosenblatt
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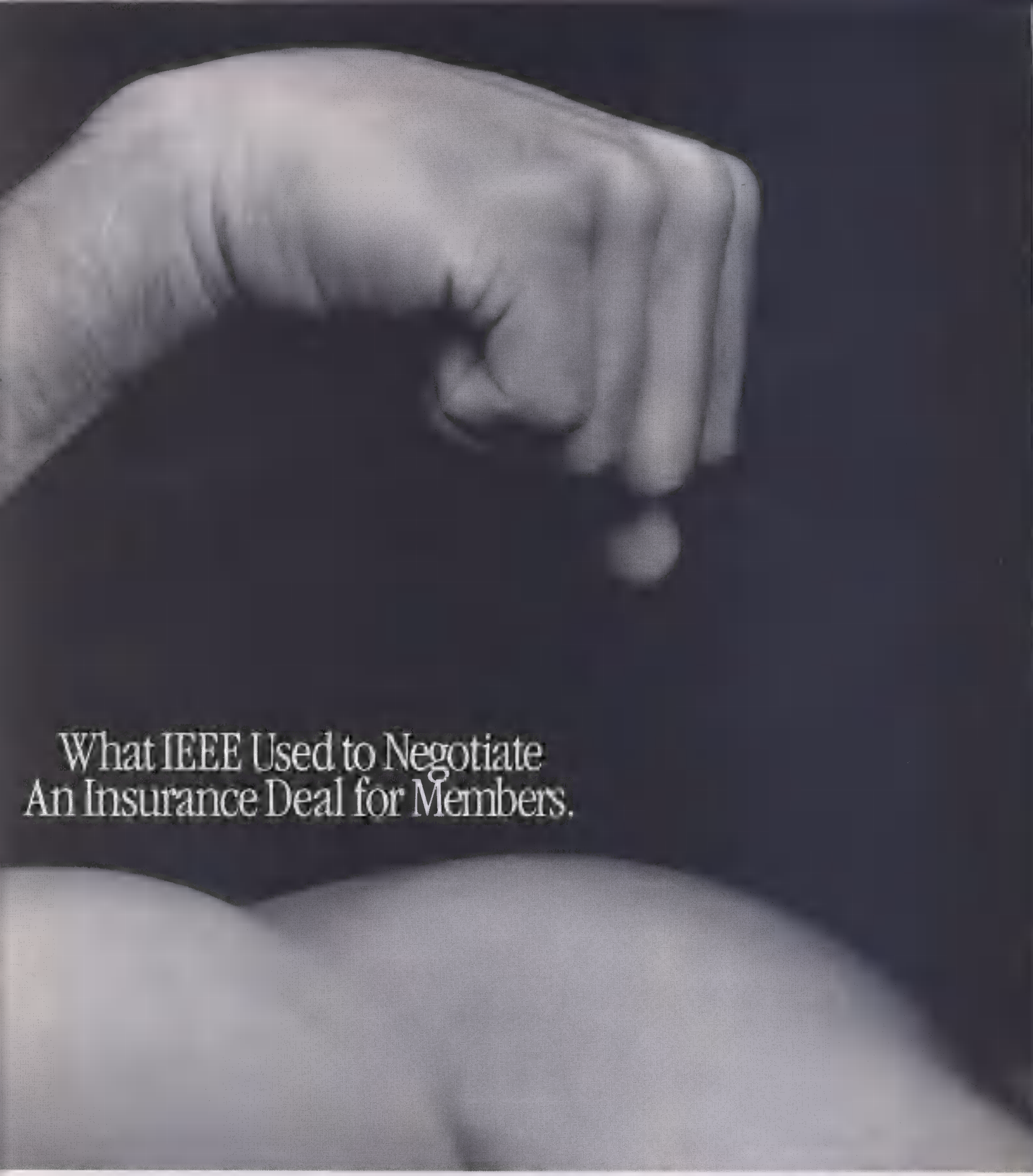
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The Institute

Congressional Fellows wanted

The competition for 1992-93 IEEE-USA Congressional Fellowships has opened in a search for at least two EEs and allied scientists who will be selected to serve a one-year term on the personal staff of either a U.S. senator or representative or on the professional staff of a Congressional committee. Additional funding sources may permit naming more than two Fellows.

Fellows will be selected on the basis of their technical competence, their ability to serve in a public environment, and their demonstration of service to the Institute and the profession. Anyone selected must be a U.S. citizen and must have been in the IEEE at Member grade or higher for at least four years.

Further information and application forms are available from W. Thomas Suttle at the IEEE-USA office, 1828 L St., N.W., Suite 1202, Washington, D.C. 20036-5104; 202-785-0017. Applications must be postmarked no later than March 31, 1992, to be eligible for consideration.

Creating disk attach standards

The IEEE Computer Society Disk Attach Study Group, headed by Martin Freeman of Philips Research, Palo Alto, Calif., and the Industry Small Form-Factor Committee, headed by Dal Allan of the consulting firm ENDL, Saratoga, Calif., are cooperating on creating a new disk interface standard for directly attaching disk drives to printed-circuit boards. In developing the new interface, the group hopes to provide a device that will link up with "disk chips," high-performance small-form-factor disk drives recently made possible by advances in head, media, servo, and digital signal-processing technologies.

The new interface will allow small-form-factor disk drives to be seen as an extended form of random-access memory chips. Disk drives thus equipped are expected to find their way into PC laptop and notebook computers, embedded applications such as laser printers and facsimile machines, and a vast array of consumer electronic equipment.

Power Society sets up new award

The Power Engineering Society (PES) has established the Walter Fee Outstanding Young Engineer Award for outstanding contributions in the leadership of technical society activities, including local and/or transnational PES and other technical societies; leadership in community and humanitarian activities; and evidence of technical competence through significant engineering achievements.

The award will be presented annually. Recipients will be given a plaque and a US $500 travel subsidy to attend the PES Summer Meeting for the award presentation. They will be asked to designate a college or university to receive a $5000 scholarship for an electrical engineering undergraduate.

Applicants must be 35 years of age or under on Jan. 1 of the presentation year and have been a member of the PES for at least one year. Nominations and applications should be directed to B. Don Russell, Walter Fee Outstanding Young Engineer Award Committee, Department of Electrical Engineering, Texas A&M University, College Station, Texas 77843-3128; 409-845-7912. The deadline is Feb. 15, 1992.

New computing publication

The Technical Activities Board has endorsed a proposal to publish the *Annals of the History of Computing* as an IEEE Computer Society periodical, beginning in 1992, and it has been approved by the IEEE Executive Committee.

Coming
in Spectrum

SOFTWARE FOR PCs AND WORKSTATIONS. The six articles in this report steer neophyte and experienced user through newly available design and data acquisition software for personal computers and workstations.

- **ASIC LOGIC SYNTHESIS.** Larger designs can now be handled in a shorter time on more platforms than before by logic synthesis packages for application-specific ICs (ASICs).
- **ELECTROMAGNETIC FIELD SOLVERS.** The success of electromagnetic field solvers on large problems will depend on the availability of massively parallel or vectorized computer hardware. Meanwhile, new solvers and new versions of old solvers have appeared.
- **DATA ACQUISITION.** Also covered will be software for data analysis and display and for technical reporting. A table will highlight significant features.
- **MATH IN PICTURES.** A good mathematics package for an engineer should solve diverse equations, support many functions, and allow graphical visualization of results.
- **EMBEDDING DSP SYSTEMS.** Embedded applications of digital signal processing raise issues like C compiler efficiency, Windows 3.0 compatibility, and size of ROM needed.
- **CASE FOR PRODUCTIVITY.** The tools of computer-aided system engineering (CASE) help the system designer automate error checking and other chores. They also engender a better understanding of the system.

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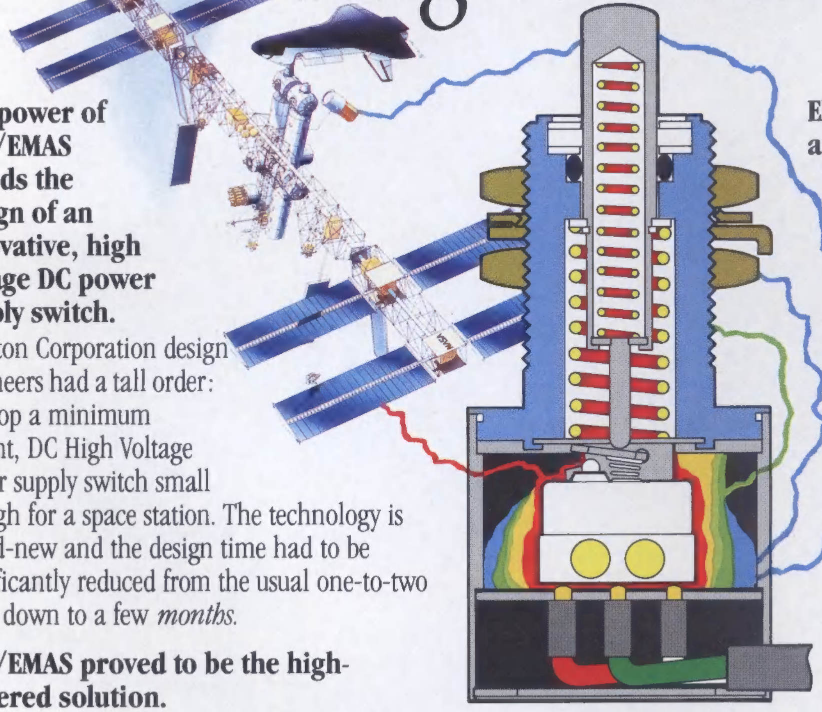

The power of MSC/EMAS speeds the design of an innovative, high voltage DC power supply switch.

Eaton Corporation design engineers had a tall order: develop a minimum weight, DC High Voltage power supply switch small enough for a space station. The technology is brand-new and the design time had to be significantly reduced from the usual one-to-two years down to a few *months.*

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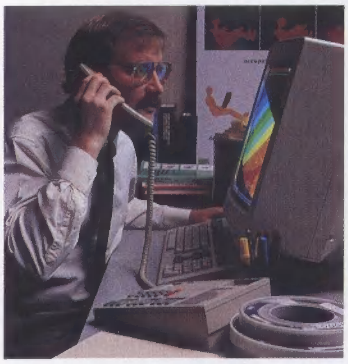

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